TABLE OF CONTENTS VOL#005 FOR 28211 001 -10991 MODE M3 RQST BY FACTORY MLC ▫▫ DATE 29JUL70

PAGE NO. SH	TITLE	PART NO. EC NO.	FEATURE B/M OR B/MS
** LOGIC TYPE	COMPONENT CIRCUITS 2		
00.00.00.0	SMS CARD CAP CODE INDEX	0826994 131802	

TOTAL PAGES THIS VOLUME 1

LOGIC NO.	MACH	SMS CARD CAP CODE INDEX	PART NO.	EC NO.
00.00.00.0	2821		0826994	131802

CARD CAP	NAME	PART NO.	REF NO.	C.E. REF NO.
1Y **	FIELD REPLACEMENT L 1	370953	370953	370953
2Y **	FIELD REPLACEMENT L 2	370954	370954	370954
3Y **	FIELD REPLACEMENT L 3	370952	370952	370952
4Y **	FIELD REPLACEMENT L 4	370951	370951	370951
5Y **	FIELD REPLACEMENT L 5	370950	370950	0370950
6Y **	FIELD REPLACEMENT L 6	370955	370955	0370955
	SDTDL FAMILY DELAY INFO 4 SHEETS			729954
AD C-	L.S. POWER TRIGGER TWIN	373316	373316	736615
AD F-	DAP SOLENOID DRIVER	372375	372375	734383
AJ T-	ALLOY DIODES TYPE AAS	370564	370564	729902
AQ N-	DJ DIODE CLAMP	370690	370690	734325
AQ Q-	GENERAL DELAY CIRCUIT	370703	370703	734340
AS Q-	ALLOY CLUTCH MAGNET DR.	372245	372245	734342
AX A-	SDTDL 4-2 WAY PLUS A WO³LOAD	372197	372197	734306
AX C-	SDTDL 1-3, 1-2 WAY -A-O 2³CARD LOAD	372202	370952	734309
AX G-	SDTDL 3-4 WAY, -A-O LOAD	372206	370951	734310
AX H-	SDTDL 4-2 WAY, 1-3 WAY -A-O LOAD	372207	370954	734313
AX K-	SDTDL 2-5 WAY -A-Q W AND WO³LOAD	372209	372209	734374
AX N-	SDTDL 3-2, -A-O 2³CARD W³O LOAD	372212	370951	734318
AX P-	SDTDL 3-4, 1-3 WAY -A-O W³O LOAD	372213	370954	734319
AX Q-	SDTDL 4-3 WAY, -A-O W³LOAD	372214	370954	734320
AX R-	SDTDL 2-2 W PLUS A PLUS O W³LOAD	372240	372240	734322
AX S-	2-2 PLUS A, PLUS O, NO LOAD	372241	372241	734323
AX V-	COMPLEMENTRY EMITTER FOLLOWER	372244	372244	734338
AX W-	SDTDL 4-3 WAY. -A-O WO³LOAD	372236	370954	734321
AX Z-	SDTDL LOW SPEED TRIGGER	372239	372239	734347
AZ K-	SDTDL SINSLE SHOT	372275	372275	734405
CE X-	1-3, 1-2 WAY -A-O W³LOAD H.S.	372530	370952	734380
CE Y-	1-3, 1-2 WAY -A-O WO³LOAD H.S.	372531	370952	734381
CE Z-	2-5 WAY -A-O DLB W OR WO³LOAD H.S.	372525	372525	734375
DE N-	SDTDL 1-6, 1-4 WAY -A W³LOAD	372195	370953	734304
DE P-	4-2 WAY PLUS AND W³LOAD	372196	372196	734305
DF J-	TDL AND TRL LOAD CARD	370232	370232	729909
DF Q-	SDTDL INVERTING POWER DRIVER	370225	370225	729910
DF R-	SDTDL NON INVERTING POWER DRIVER	370226	370226	729911
DG C-	SDTDL MEMORY .150 USEC DELAY LINE	370244	370244	734348
DG D-	SDTDL MEMORY .280 USEC DELAY LINE	370245	370245	734349
DG F-	SDTDL MEMORY .525 USEC DELAY LINE	370247	370247	734351
DG H-	SDTDL MEMORY 1.2 USEC DELAY LINE	370249	370249	734352
DG S-	SDTDL INDICATOR DRIVER	370347	370347	729912
DG T-	SDTDL 2 WAY LOGIC BLCK LOW SP W LDS	370380	370380	729913
DG U-	SDTDL 2 WAY LOGIC BLK LOW SP W³O LDS	370379	370379	729914
DG V-	SDTDL 2 WAY LOGIC BLCK LOW SP W LDS	370378	370378	729915
DG W-	SDTDL 3 WAY LOGIC BLK LOW SP W³O LD	370377	370377	729916
DG X-	SDTDL 5 WAY LOGIC BLCK LOW SP W LDS	370376	370953	729917
DG Y-	SDTDL 5 WAY LOGIC BLK LOW SP W³O LD	370375	370953	729918
DG Z-	SDTDL 10 WAY LOG BLK LOW SP W LOAD	370373	370955	729919
DH B-	SDTRL INVERTER LOW SPEED WITH LOAD	370348	370950	729921

LOGIC NO.	MACH	SMS CARD CAP CODE INDEX	PART NO.	EC NO.
00.00.00.0	2821		0826994	131802

CARD CAP	NAME	PART NO.	REF NO.	C.E. REF NO.
DH C-	SDTDL INVERTER LOW SPEED W/O LOAD	370372	370950	729922
DH F-	SDTDL TRIGGER AND DRIVER	370350	370350	729925
DH J-	SDTDL MUP NUMBER 4	370352	370352	729928
DH V-	SDTDL 1-6, 1-4 WAY -A W/LOAD	372123	370953	734301
DH W-	SDTDL LATCH 3/CARD	372191	372191	734354
DH Y-	SDTDL 1-8, 1-2 WAY -A W/LOAD	372193	370953	734302
DJ A-	BUFFER MATRIX SWITCH CARD	373329	373329	373329
DJ B-	BUFFER MEMORY CARD	373330	373330	373330
DJ L-	SDTDL SINGLE SHOT HAMMER DR.	373354	373354	734404
DK J-	SDTDL RELAY DRIVER LATCHING	372473	372473	734387
DK Q-	DIFFERENCE AMPLIFIER	372496	372496	734390
DK R-	INHIBIT DRIVER	372497	372497	734442
DK S-	1330 KC OSCILLATOR + SHAPER	372501	372501	734373
DK T-	1600 KC OSCILLATOR + SHAPER	372500	372500	734372
DK U-	SDTDL INTEGRATOR	372508	372508	734420
DK W-	POWER LATCH H.S.	372526	372526	734376
DK X-	4-3 WAY -A-O W/LOAD H.S.	372527	370954	734377
DK Y-	1-6, 1-4 WAY -A W/LOAD H.S.	372528	372528	734378
DK Z-	3-4 WAY -A-O W/LOAD H.S.	372529	370951	734379
ED Z-	6 VOLT AMPLIFIER CARD FOR MPS	374621	374621	374621
ES G-	SPD-CURRENT DRIVE	374907	374907	837973
ES X-	INDICATOR DRIVER	374924	374924	374924
FP Z-	STACKER RATE LIMITER	375157	375157	849091
FR H-	STD INTF LINE REC + GATED LINE DRVR	375188	375188	2532396
FR N-	SELECT-OUT SEQUENCE CARD	375193	375193	2532397
HF T-	SDTDL HS TRIGGER	372575	372575	734333
HG A-	ROW BIT	373373	373373	734417
JE A-	LINE REC-SLT TO NAND,NAND TO SLT	374791	374791	846924
JE B-	VOLTAGE SEQUENCING CARD	374792	374792	374792
UG R-	SENSE AMP DECTECTOR	372992	372992	743068
UG T-	NON INVERTING SIMPLEX LINE DRIVER	372976	372976	822929
Y3 --	JUMPER CARD ADDRESSING	370858	370858	370858
YK R-	SDTDL DATA REG. AND INHBT DRIVER	372220	372220	734392
YK S-	SDTDL ADDRESS REGISTER	372221	372221	734393
YK T-	BIAS LOAD	372222	372222	734394
YK U-	SET/RESET LOAD	372223	372223	734395
YK V-	INHIBIT LOAD	372224	372224	734396
YK W-	VOLTAGE REGULATOR L2	372225	372225	734397
YK X-	VOLTAGE REGULATOR L3	372226	372226	734398
YK Y-	PARTIAL VOLT. REG. + SENSE GATE GEN.	372227	372227	734399
YL A-	SENSE AMPLIFIER	372229	372229	734401
YP M-	REED RELAY	372680	372680	372680
YY A-	CORE INTERFACE	372701	372701	822942
YY B-	EMITTER GATE FOLLOWER	372702	372702	822940
YY C-	CAPACITOR CABLE CARD	372719	372719	372719
YY D-	CORE MATRIX CARD	373432	373432	822938
YY N-	SDTDL-SDTRL INTERFACE TERM GATED	372723	372723	822935
Z6 G-	SDTDL FOUR 2 WAY N AND LOG BCKS W LD	372585	372585	734339
Z6 H-	SDTDL 4 2 WAY N AND LOG BLKS W/O LDS	372586	372586	734341
Z6 J-	SDTDL 3 WAY N AND LOG BLK W/LOADS	372587	372587	734366

LOGIC NO.	MACH	SMS CARD CAP CODE INDEX	PART NO.	EC NO.
00.00.00.0	2821		0826994	131802

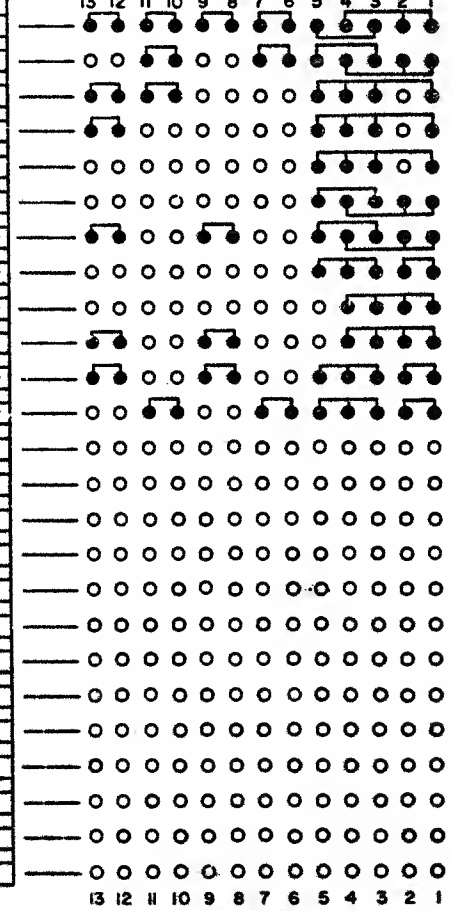
CARD CAP	NAME	PART NO.	REF NO.	C.E. REF NO.
Z6 K-	SDTDL 3 WAY N AND LOG BLK W/O LDS	372588	372588	734402
Z6 L-	SDTDL 2-5 WAY N AND LOG BLK W/LOADS	372589	370953	734367
Z6 M-	SDTDL 2-5 WAY N AND LOG BLK W/O LDS	372590	370953	734366
Z6 N-	SDTDL ONE 10 WAY LOGIC BLOCK	372591	370955	734368
ZG P-	SDTDL LOGIC INV. HS LOAD	372592	370956	734369
Z6 Q-	SDTDL LOGIC INV. HS WO/LOAD	372593	370956	734370
ZK T-	720KC OSCILLATOR AND SHAPER	372682	372682	734384
ZU D-	12 VOLT AMPLIFIER CARD FOR MPS	372085	372085	372085

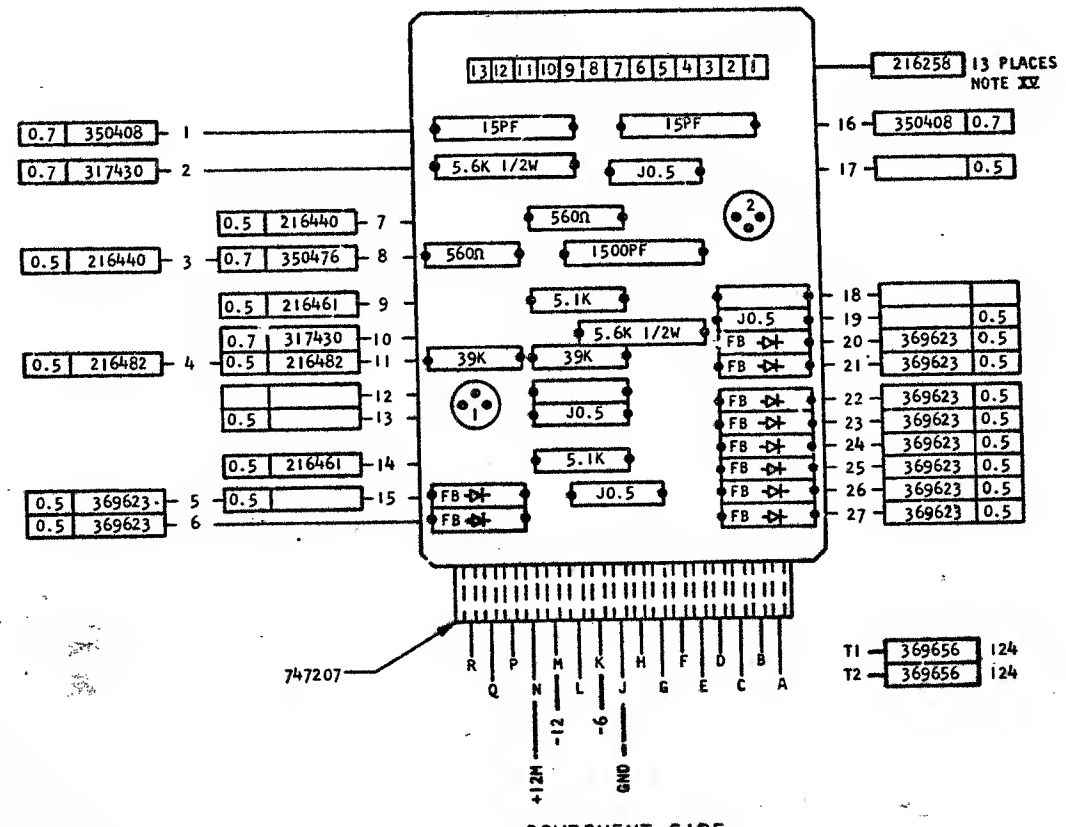
CARD CODE	STANDARDS CODE	370953
1Y **	2-7045	

FIELD USE

CAP CONFIGURATION

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC	CARD CODE
2-5 WAY (-A) LOADS	KM	372589	870585	ZGL-
2-5 WAY (-A) WITHOUT LOADS	KE	372590	870585	ZGM-
1-10 WAY (-A)	KH	372591	870585	ZGN-
10 WAY LOGIC BLOCK LOW SPEED W/LOAD	KA	370373	892380	DGZ-
10 WAY LOGIC BLOCK LOW SPEED WO/LOAD	KB	370374	892380	DHA-
5 WAY LOGIC BLOCK LOW SPEED W/O LOAD	KG	370375	892380	DGY-
5 WAY LOGIC BLOCK LOW SPEED W/ LOAD	KF	370376	892380	DGX-
1-6 WAY, 1-4 WAY WO/LOAD (-A)	KL	372123	892216	DHV-
1-8 WAY AND 1-2 WAY WO/LOAD	KC	372193	892216	DHY-
1-8 WAY AND 1-2 WAY W/LOAD	KJ	372194	892380	DHZ-
1-6 WAY, 1-4 WAY W/LOAD (-A)	KK	372195	892380	DEN-
1-6 WAY, 1-4 WAY(-A) WO/LOAD H.S.	KD	372528	892216	DKY-



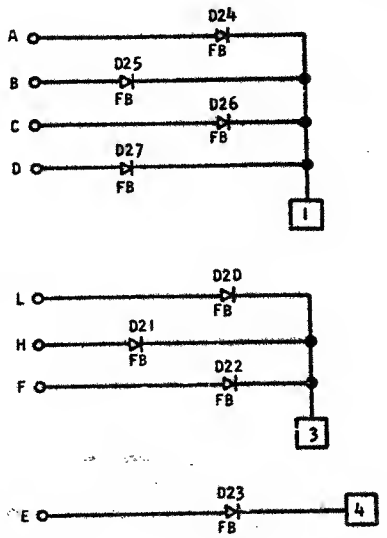


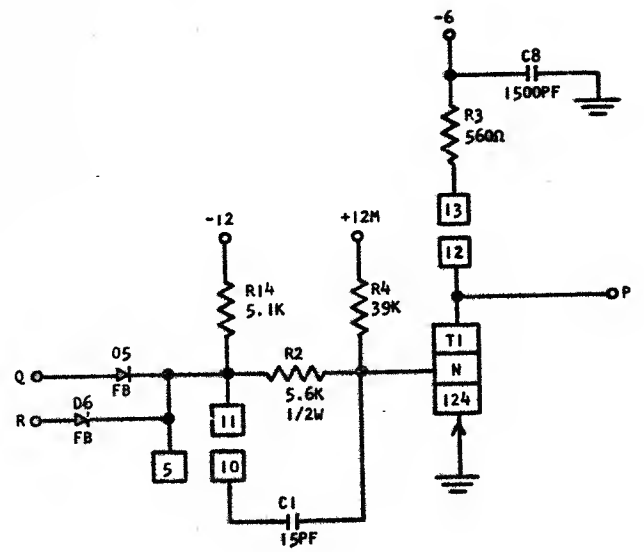
COMPONENT SIDE

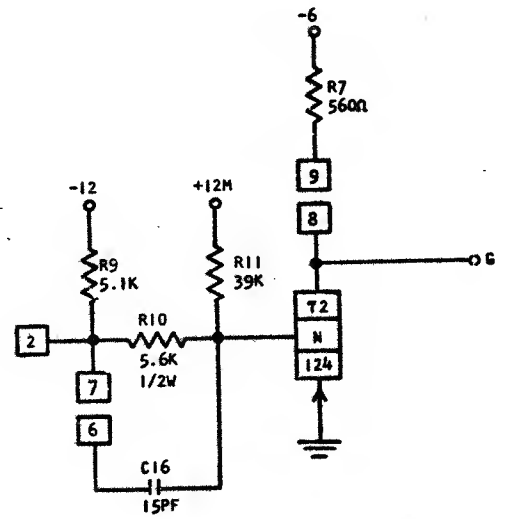
FIELD REPL CARD WITH PLUGGABLE CAP

NOTES

- X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION
- XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
- XII ALL RESISTORS ARE 1/4 WATT AND ±5% UNLESS OTHERWISE NOTED
- XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491296
- XIV POSITIONS T1 AND T2 ARE TO-18 TRANSISTORS WHICH MAY BE MOUNTED ON .100 OR .200 PIN CIRCLE HOLES. USE TRANSISTOR SPACER 483070 FOR .200 PIN CIRCLE MOUNTING
- XV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE







C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
ABC GS	3-5-63

370553

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPRUVAL	DEVELOPMENT NO.	370553
NAME CARD ASM TSTR- FIELD						4-16-63	116160	EHR				X1322B	
REPL. CARD WITH PLUGGABLE CAP													
HOLE PATTERN	DESIGN			TYPE	SMS 1441								
	DETAIL			SCALE	NONE							CIRCUIT FAMILY	
490369	CHECK	LIG	3-14-63	DRAW	LIG 3-14-63							SOTOL	
	APPRO	GWS	4-16-63	CHECK	TMG 13-26-63								

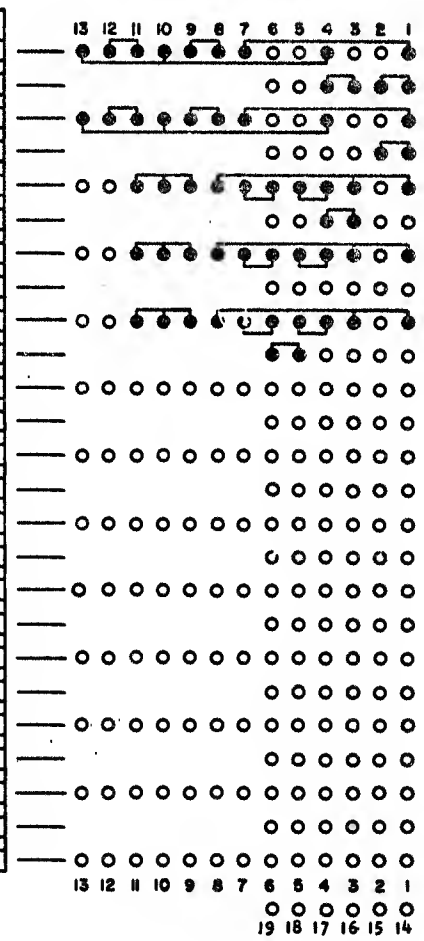
2-2

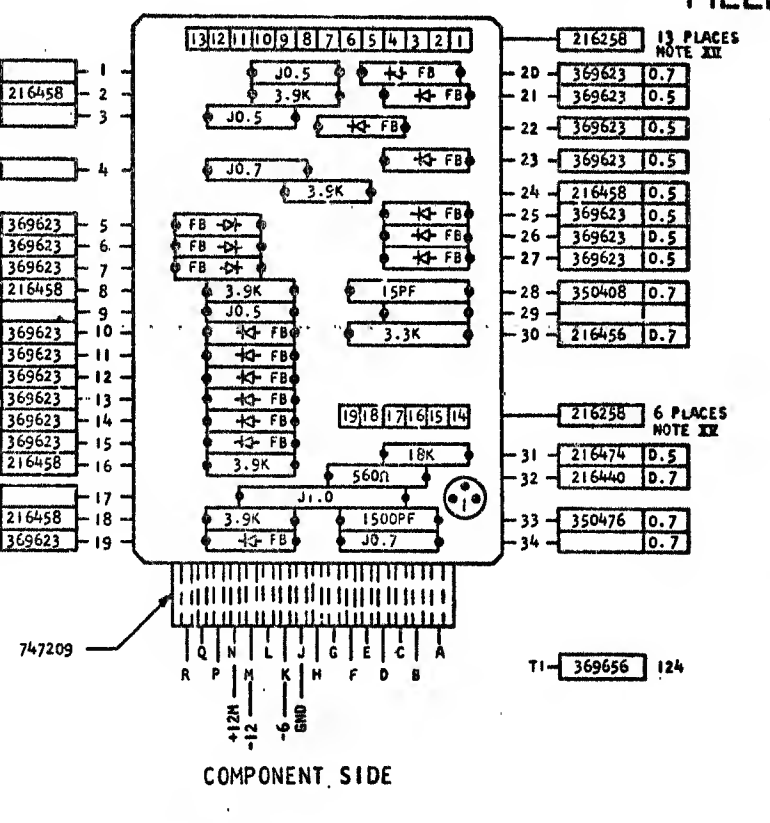
CARD CODE	STANDARDS CODE	370954
2Y **	2-7046	

FIELD USE

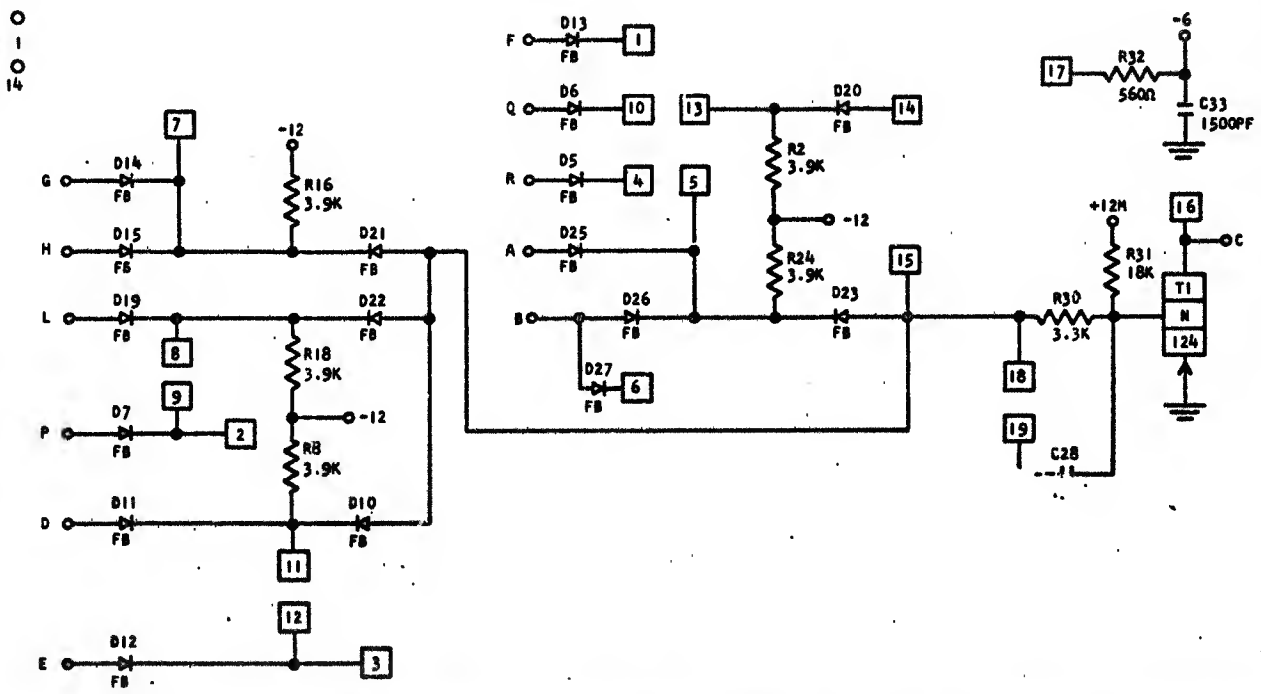
CAP CONFIGURATION

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC	CARD CODE
4-2 WAY, 1-3 WAY (-A,-0)	KN	372207	870201	AXH-
4-2 WAY, 1-3 WAY (-A,-0) WO/LOAD	KP	372213	870201	AXP-
4-3 WAY (-A,-0) W/LOAD - SDTDL	KQ	372214	870201	AXQ-
4-3 WAY (-A,-0) WO/LOAD - SDTDL	KR	372236	870201	AXW-
4-3 WAY (-A,-0) WO/LOAD H.S.	KS	372527	870529	OXX-





COMPONENT SIDE



NOTES

X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION
XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
XII ALL RESISTORS ARE 1/4 WATT AND ±5% UNLESS OTHERWISE NOTED
XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296
XIV POSITION T1 IS A TO-18 TRANSISTOR WHICH MAY BE MOUNTED IN .100 OR .200 PIN CIRCLE HOLES. USE TRANSISTOR SPACER 483070 FOR .200 PIN CIRCLE MOUNTING
XV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

FIELD REPL CARD WITH PLUGGABLE CAP

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
ABC GS	3-5-63

370954

HOLE PATTERN 490370

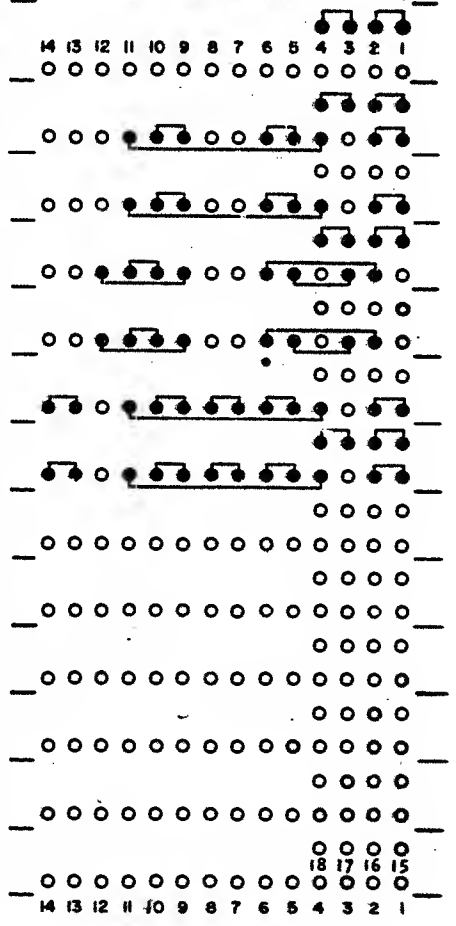
INTERNATIONAL BUSINESS MACHINES CORP.													
NAME	CARD ASM TSTR-FIELD REPL CARD WITH PLUGGABLE CAP					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	370954
						A-16-63	116160	[illegible]				X1326B	
DESIGN				TYPE	SMS 1441								
DETAIL				SCALE	NONE								
CHECK	LIG	5-15-63	DRAW	LIG	3-15-63							CIRCUIT FAMILY	
APPRO	GWS	5-16-63	CHECK	KRB	3-26-63							SDTDL	

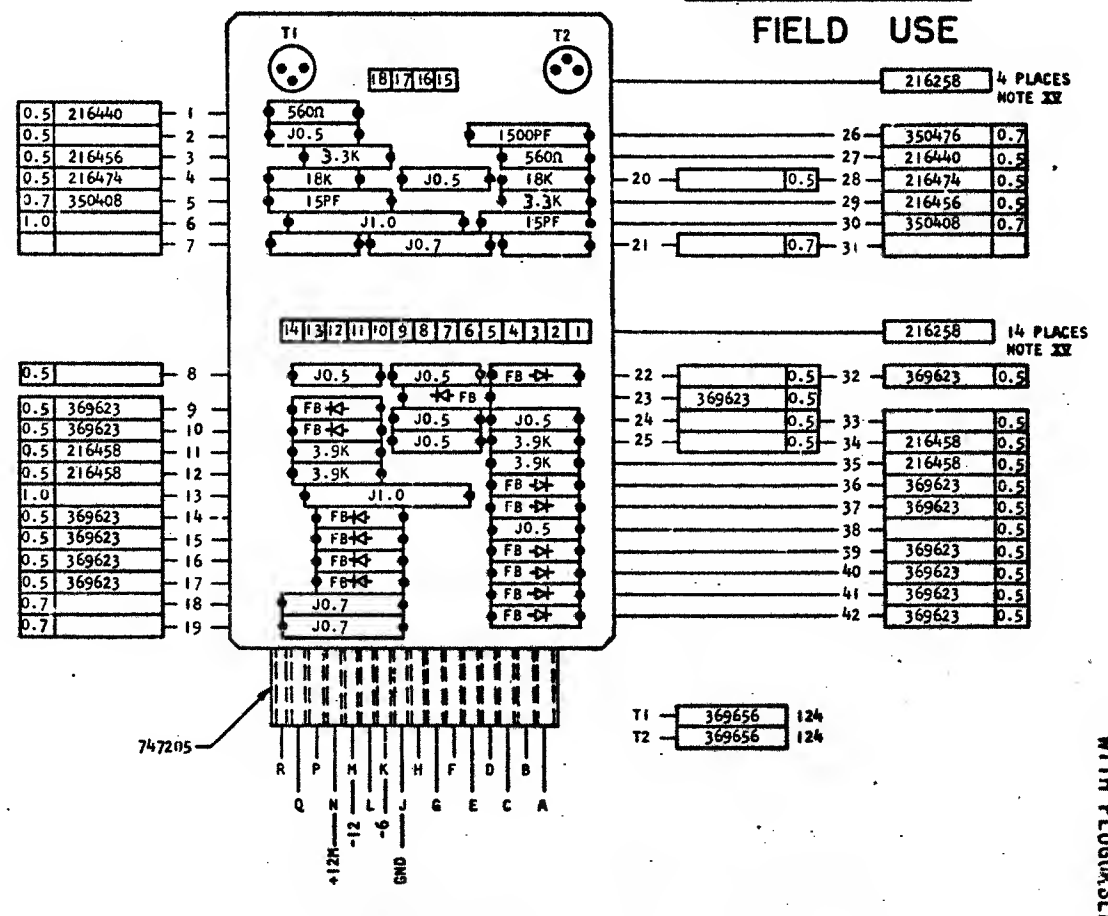
CARD CODE	STANDARDS CODE	370952
3Y **	2-7045	

FIELD USE

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC	CARD CODE
2-2 WAY, 2/CARD (-A,-0)	KT	372201	870201	AXB-
1-2 WAY, 1-3 WAY 2/CARD (-A,-0)	KU	372202	870201	AXC-
1-2 WAY, 1-3 WAY (-A,-0) WO/LOAD	KV	372208	870201	AXJ-
2 OBL 2(2W-A)-OR EXT	KW	372204	870201	AXE-
2 DBL 2(2W-A)-OR EXT WO/LOAD	KX	372210	870201	AXL-
1-3 WAY, 1-2 WAY(-A-0)WO/LOAD H.S.	KY	372531	870529	CEY-
1-3 WAY, 1-2 WAY(-A-0)W/LOAD H.S.	KZ	372530	870529	CEX-

CAP CONFIGURATION





COMPONENT SIDE

FIELD REPLACEMENT CARD WITH PLUGGABLE CAP

NOTES

X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION

XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999

XII ALL RESISTORS ARE 1/4 WATT AND ±5% UNLESS OTHERWISE NOTED

XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296

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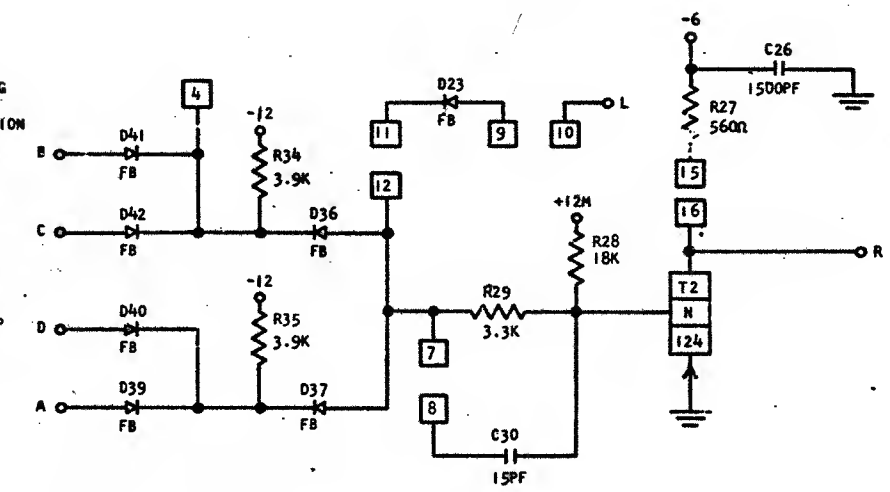
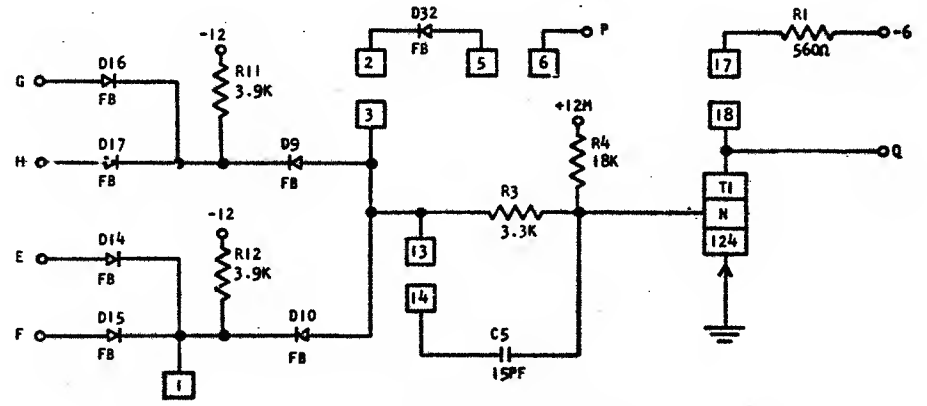
XV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE





C

DPO CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
ABC GS	3-5-63

370952

HOLE PATTERN 490368

INTERNATIONAL BUSINESS MACHINES CORP.												
NAME	CARD ASM TSTR--FIELD REPL CARD WITH PLUGGABLE PROG CAP					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
						4-16-63	116160	[illegible]				X1306-B
						6-19-63	D117810	MDL				
DESIGN			TYPE	SMS 1411								
DETAIL			SCALE	NONE								
CHECK	LIG	3-19-63	DRAW	LIG	3-19-63							CIRCUIT FAMILY
APPRO	GVS	4-16-63	CHECK	[illegible]	3-26-63							SDTDL

370952

2-2

CARD CODE	STANDARDS CODE	370951
4Y **	2-7045	

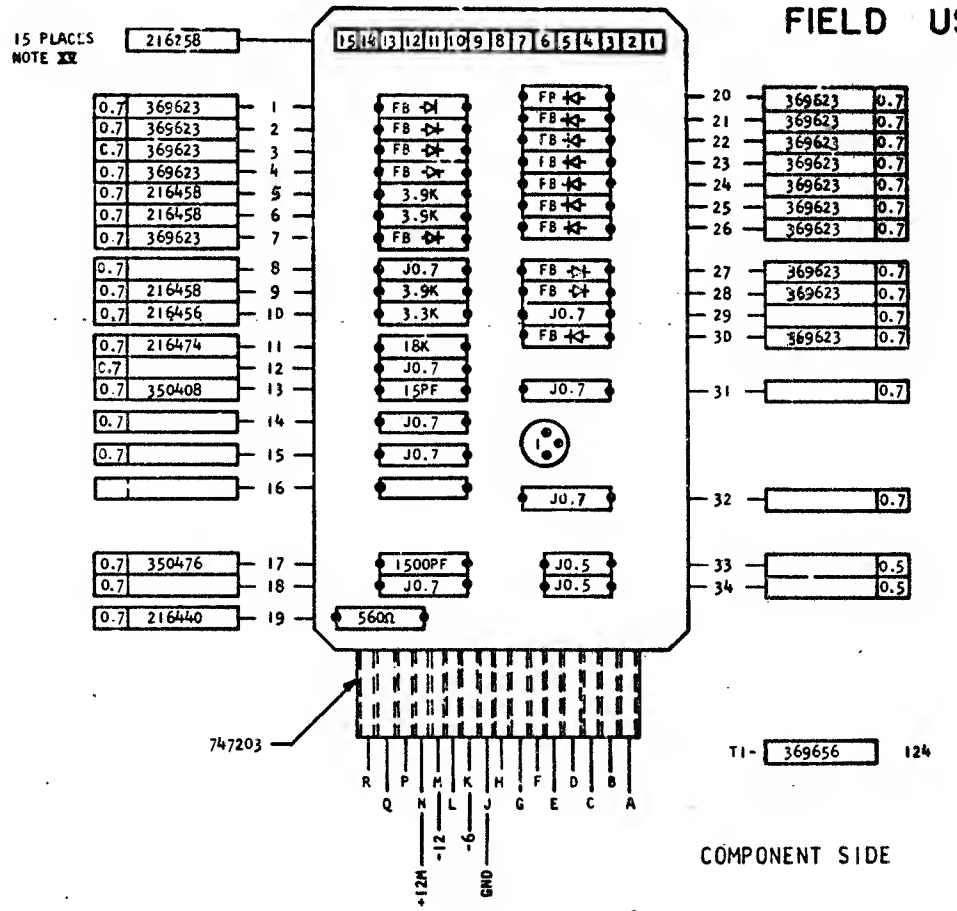
CAP CONFIGURATION

CIRCUIT NAME	CAP CODE	ASM. NO	TEST SPEC	CARD CODE
3-4 WAY LOAD (-A, -0)	JN	372206	870201	AXG-
3-4 WAY W/O LOAD (-A, -0)	JP	372212	870201	AXN-
3-4 WAY (-A, -0) W/O LOAD H.S.	JQ	372529	870529	OKZ-

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

FIELD USE

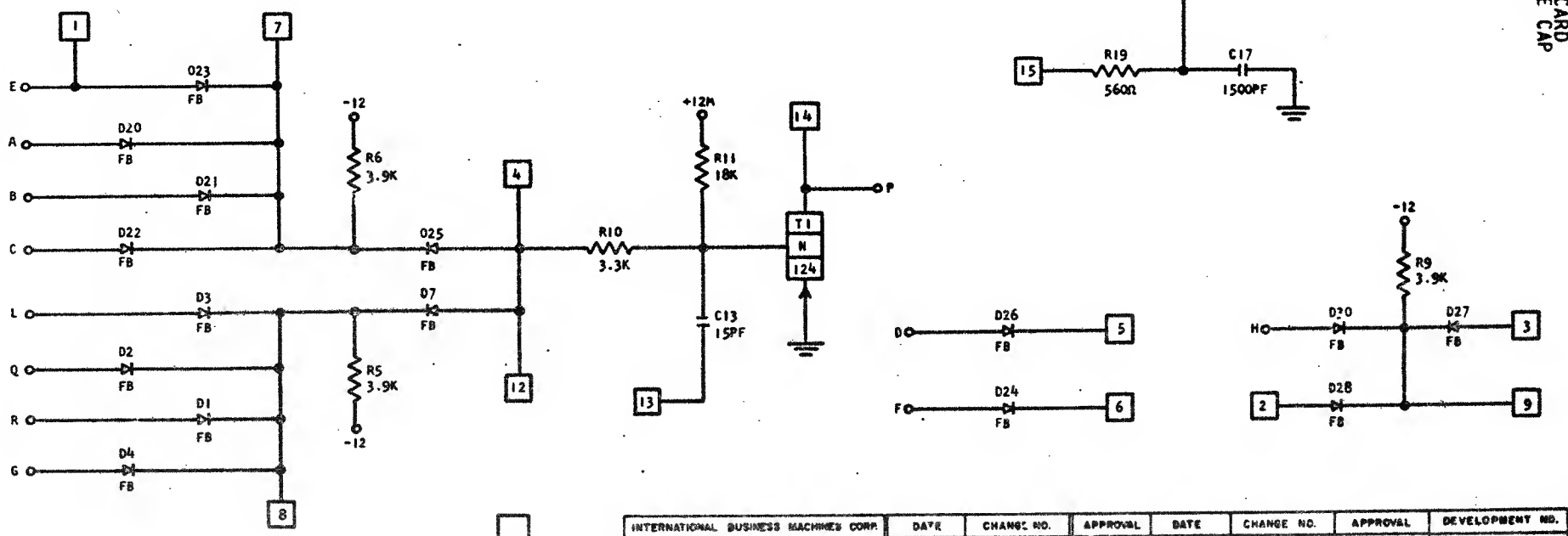


COMPONENT SIDE

FIELD REPL CARD WITH PLUGGABLE CAP

NOTES

- X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION
- XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
- XII ALL RESISTORS ARE 1/4 WATT AND ±5% UNLESS OTHERWISE NOTED
- XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296
- XIV POSITION T1 IS A TO-18 TRANSISTOR WHICH MAY BE MOUNTED IN .100 OR .200 PIN CIRCLE HOLES. USE TRANSISTOR SPACER 483070 FOR .200 PIN CIRCLE MOUNTING
- XV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE



C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
ABC GS	3-5-63

370951

HOLE PATTERN 490367

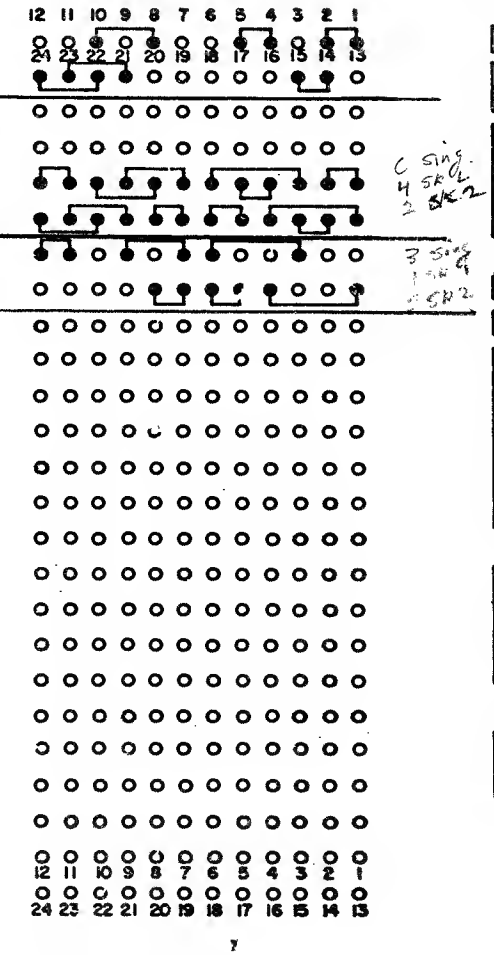
INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR - FIELD				4-16-63	116160	ZMR				X1304B
REPL CARD WITH PLUGGABLE CAP										
DESIGN			TYPE SMS 1481							
DETAIL			SCALE NONE							
CHECK LJG 4-18-63			DRAW LTG 4-18-63							CIRCUIT FAMILY
APPRO GWS 4-16-63			CHECK [illegible] 13 APR 63							SDTDL

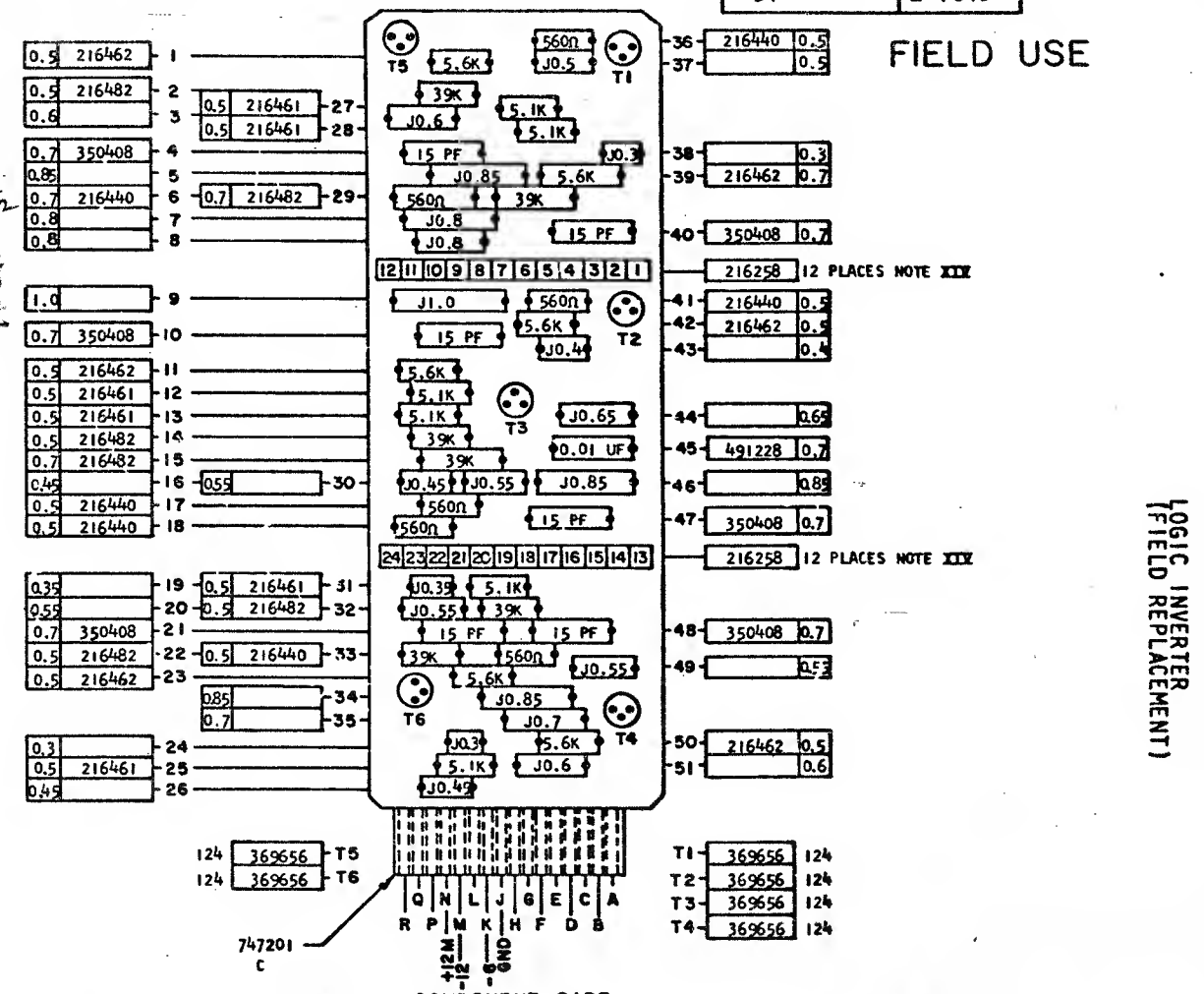
370951

CARD CODE	STANDARDS CODE	370950
5Y**	2-7045	

CIRCUIT NAME	CAP CODE	ASM NO.	TEST SPEC	CARD CODE
INVERTER LOW SPEED WITH LOAD	JR	370348	892380	0HB-
NVERTER LOW SPEED WITHOUT LOAD	--	370372	892380	0HC-
H.S. LOGIC INVERTER	JS	372552	870585	ZGP-
H.S. LOGIC INVERTER WITHOUT LOADS	JT	372593	870585	ZGQ-

CAP CONFIGURATION





FIELD USE

LOGIC INVERTER (FIELD REPLACEMENT)

COMPONENT SIDE

NOTES

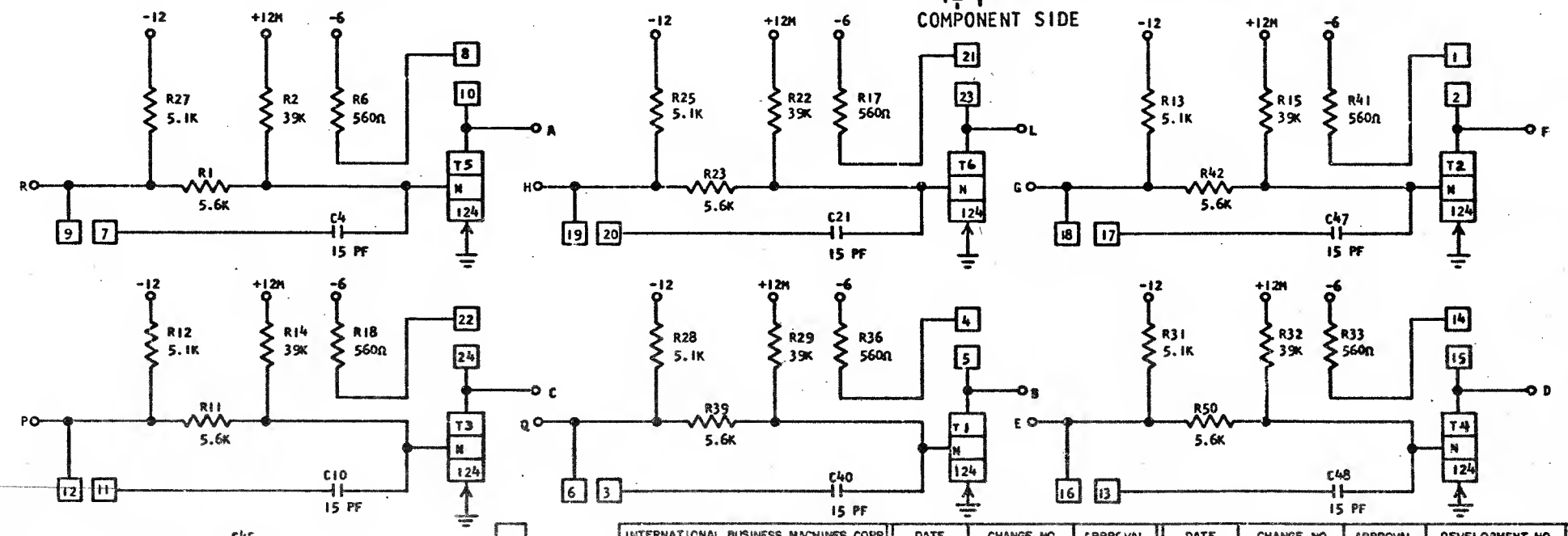
I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION

II ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999

III "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296

IIII ALL RESISTORS ARE 1/4 WATT AND ±5% UNLESS OTHERWISE NOTED

IIIV REFERENCE 216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE.



MFG ENG		
DPO CIRCUIT & PACKAGING STANDARD		
APPROVAL	DATE	
ABC (GS)	5MAR63	

370950

INTERNATIONAL BUSINESS MACHINES CORP.

NAME CARD ASM TSTR-LOGIC INVERTER (FIELD REPLACEMENT)

HOLE PATTERN							
490366	DESIGN	VE	10OCT67	TYPE	SMS 1441		
	DETAIL	VE	10OCT67	SCALE	NONE		
	CHECK	VE	10OCT67	DRAW	VE	10OCT67	
	APPRO			CHECK			

DATE	CHANGE NO.	APPROVAL
16APR63	116160	LHR
7FEB66	126401E	LRF
21OCT66	D130355	JCK
24OCT67	0132152	AWS

DATE	CHANGE NO.	APPROVAL

DEVELOPMENT NO. X1283B

CIRCUIT FAMILY SDTDL

370950

2-1

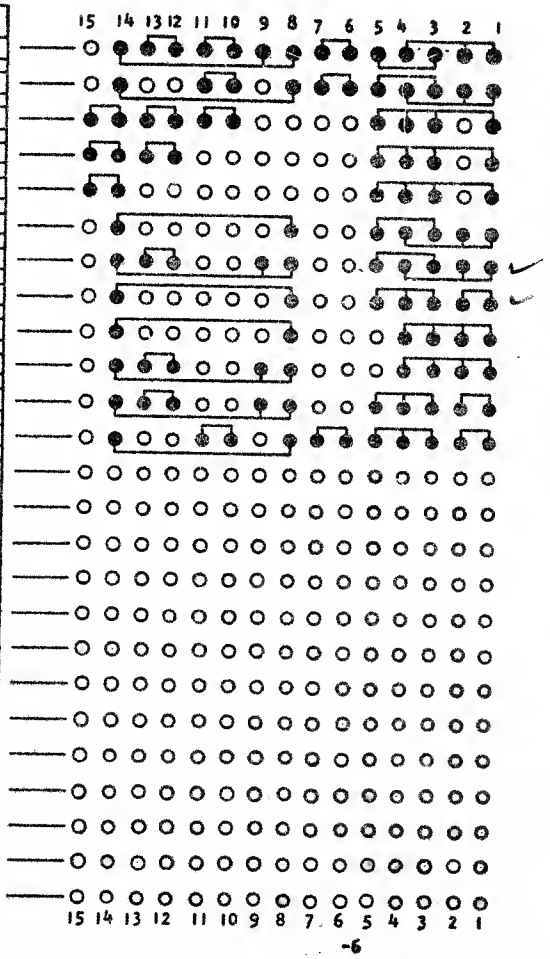
FIELD REPL. CARD WITH PLUGGABLE CAP

370955

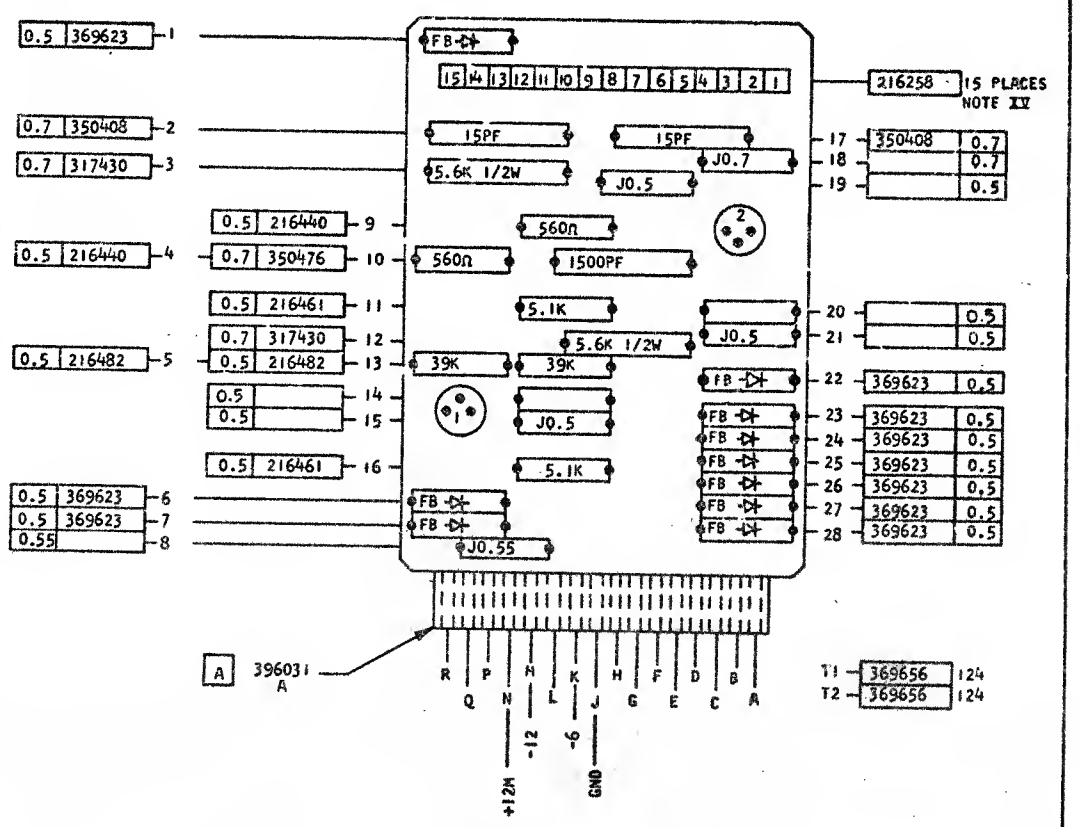
STANDARDS CODE 2-7045

CIRCUIT NAME	CAP CODE	ASM. NO	TEST SPEC	CARD CODE
2-5 WAY (-A) LOADS	JU	372589	870585	ZGL-
2-5 WAY (-A) WITHOUT LOADS	JV	372590	870585	ZGM-
1-10 WAY (-A)	JW	372591	870585	ZGN-
10 WAY LOGIC BLOCK LOW SPEED W/LOAD	JX	370373	892380	OGZ-
10 WAY LOGIC BLOCK LOW SPEED WO/LOAD	JY	370374	892380	OHA-
5 WAY LOGIC BLOCK LOW SPEED WO/LOAD	JZ	370375	892380	DGY-
5 WAY LOGIC BLOCK LOW SPEED W/LOAD	JM	370376	892380	DGX-
1-6 WAY. 1-4 WAY WO/LOAD (-A)	LW	372123	892216	DHV-
1-8 WAY AND 1-2 WAY WO/LOAD	LX	372193	892216	DHY-
1-8 WAY AND 1-2 WAY W/LOAD	LY	372194	892380	DHZ-
1-6 WAY. 1-4 WAY W/LOAD (-A)	LZ	372195	892380	DEN-
1-6 WAY. 1-4 WAY (-A) WO/LOAD H.S.	MZ	372528	892216	DKY-

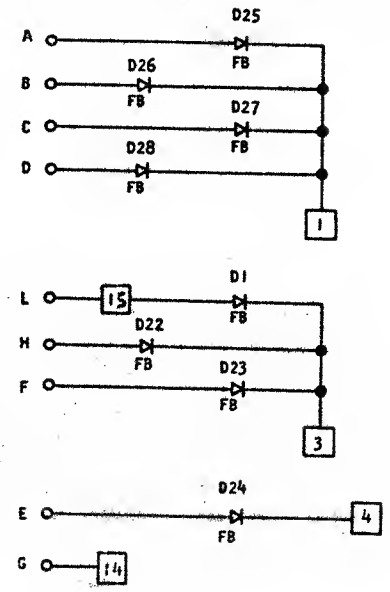
CAP CONFIGURATION

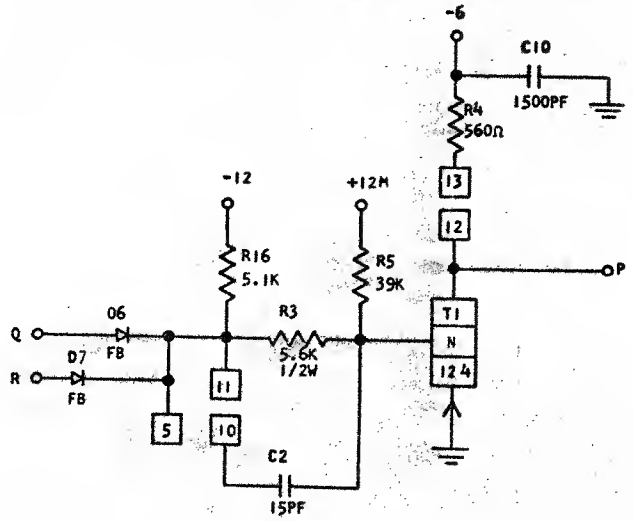


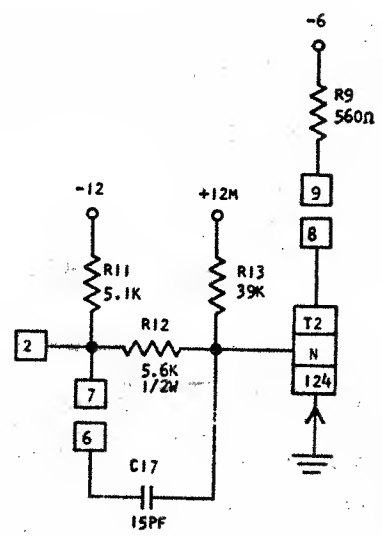
FIELD USE



COMPONENT SIDE







NOTES
- X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION
- XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
- XIII ALL RESISTORS ARE 1/4 WATT AND ±5% UNLESS OTHERWISE NOTED
- XIIII "J" IN BLOCK DENOTES BARE WIRE JUMPER. 491296
- XIV POSITIONS T1 AND T2 ARE TO-18 TRANSISTORS WHICH MAY BE MOUNTED ON .100 OR .200 PIN CIRCLE HOLES. USE TRANSISTOR SPACER 483070 FOR .200 PIN CIRCLE MOUNTING
- XV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

CARD CODE 6 y * *

370955

370955 HOLE PATTERN 747858

INTERNATIONAL BUSINESS MACHINES CORP.

	NAME	DATE
DESIGN	CARD ASM TSTR-FIELD REPL. CARD WITH PLUGGABLE CAP	5-15-64
DETAIL	MODEL SMS 1441	8-6-64
CHECK	SCALE NONE	
APPRO	DRAWN VE 4-23-64	
CHECK	CHECK	

CHANGE NO.	APPROVAL	DATE
121027		5-15-64
D121668	FVL	8-6-64

CIRCUIT FAMILY SDTDL

DEVELOPMENT NO. 370955

CIRCUIT AND PACKAGING STANDARD APPROVAL DATE 5/11/64

FORM 88-001

STANDARDS CODE

729954

CARD CODE 729954

SDTDL LOGIC FAMILY DELAY INFORMATION

GENERAL

THE TURN ON, TURN OFF DELAYS OF THE CIRCUITS USED IN A PARTICULAR MACHINE ARE COMPLEX FUNCTIONS OF MANY VARIABLES SUCH AS THE TRANSISTOR DELAY, INPUT-OUTPUT LOADING, FALL AND RISE TIME, ETC.

THE DELAY SPECIFICATIONS ARE GIVEN BELOW AND ARE CLASSIFIED BY CIRCUIT TYPE.

WHEN POSSIBLE, REPRESENTATIVE RANGES OF DELAYS ARE GIVEN ON EACH INOIVIDUAL CIRCUIT SHEET AND SHOULD BE USED AS A GUIOE. SPECIFIC CIRCUIT APPLICATION ANO/OR CAPACITIVE LOAD (EXAMPLE: WIRE CAPACITANCE) MAY RESULT IN OELAYS WHICH ARE OUT OF THE GIVEN RANGES.

THE FOLLOWING INFORMATION IS PROVIOED FOR THOSE CASES WHERE CARO REPLACEMENT DOES NOT RESULT IN IMPROVEMENT AND A MORE OETAILEO ANALYSIS IS NECESSARY.

HIGH SPEEO, LOW SPEED CIRCUITS

THE SDTDL CIRCUITS ARE CLASSIFIEO INTO TWO MAJOR FAMILIES, THE LOW SPEEO AND THE HIGH SPEED CIRCUITS. THE OIFFERENCE BETWEEN THE TWO FAMILIES CONSISTS OF THE INPUT SPEED UP CAPACITOR THAT IS USED ONLY IN THE HIGH SPEED LOGIC BLOCKS.

DELAY CHARTS:

NUMEROUS CHARTS GIVING OELAY INFORMATION HAVE BEEN INCLUDED IN THIS DOCUMENT. BOTH MINIMUM AND MAXIMUM DELAYS ARE GIVEN AS A FUNCTION OF SOME VARIABLE OR VARIABLES. NOMINAL DELAYS HAVE BEEN AVOIDED DUE TO POSSIBLE MISINTERPRETATIONS. THE MAXIMUM DELAYS GIVEN ARE SLIGHTLY LESS THAN THE THEORETICAL MAXIMUM OELAY. THE MAXIMUM OELAYS GIVEN SHOULD NOT BE EXCEEOEO IN PRACTICAL APPLICATIONS.

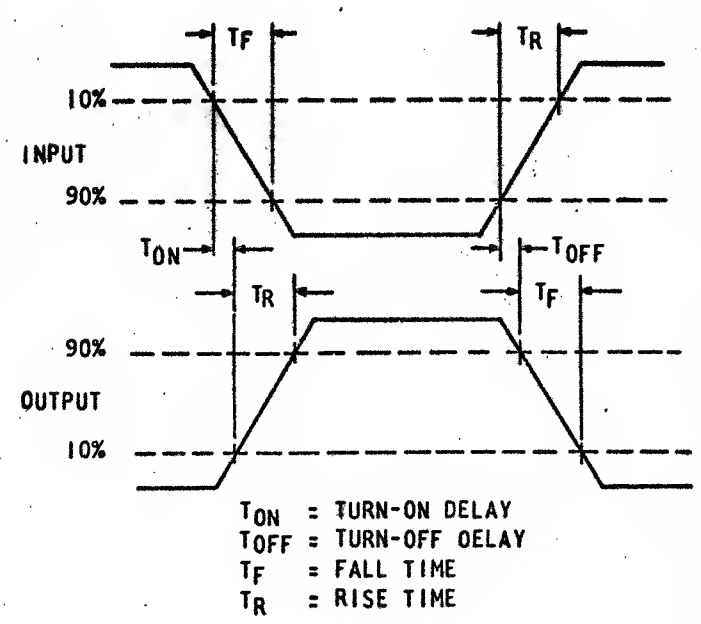
USE OF GRAPHS

THE FOLLOWING STEPS ARE RECOMMENOED FOR USING THE INFORMATION PROVIOED IN THE ACCOMPANYING GRAPHS.

1. GIVEN A LOAD CONFIGURATION REFER TO THE GRAPH OUTPUT FALL TIME VS. LOADING TO OETERMINE THE OUTPUT FALL TIME.
2. GIVEN THE INPUT FALL TIME, THE OUTPUT RISE IS DETERMINED FROM THE GRAPH OF OUTPUT RISE TIME VS. INPUT FALL TIME.
3. KNOWLEOGE OF THE RISE TIME ANO USE OF THE GRAPH OF TURN-OFF DELAY VS. INPUT RISE TIME RESULTS IN TURN-OFF LIMITS.
4. KNOWLEDGE OF INPUT FALL TIME AND USE OF THE GRAPH OF TURN-ON DELAY VS. INPUT FALL TIME RESULTS IN TURN-ON LIMITS.

DEFINITIONS

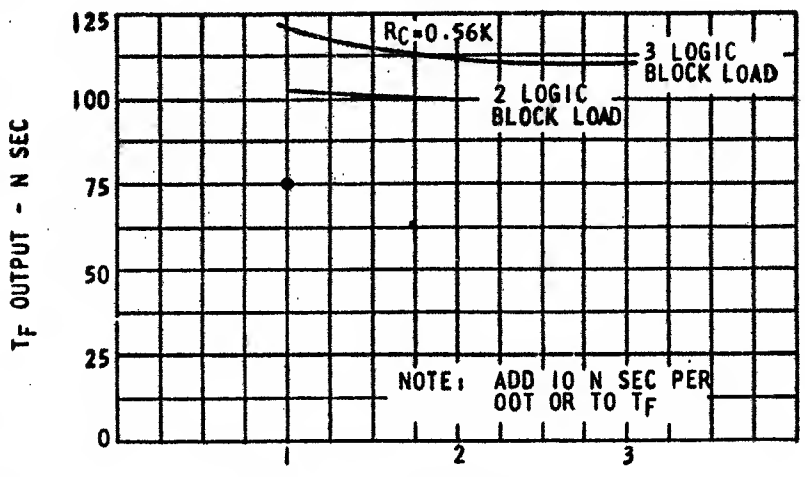
THE RISE ANO FALL TIMES WERE MEASURED FROM THE 10% TO 90% POINTS OF THE INPUT AND OUTPUT WAVEFORM. THE TURN-ON DELAY WAS MEASURED AS THE TIME INTERVAL BETWEEN 10% OOWN AT THE INPUT TO 10% UP AT THE OUTPUT. THE TURN-OFF DELAY WAS MEASURED AS THE TIME INTERVAL BETWEEN 10% UP AT THE INPUT TO 10% DOWN AT THE OUTPUT. UNLESS OTHERWISE STATED THE RISE, FALL AND DELAY TIMES ARE GIVEN IN N SEC (NANOSECONDS).



T_{ON} = TURN-ON DELAY
T_{OFF} = TURN-OFF OELAY
T_F = FALL TIME
T_R = RISE TIME

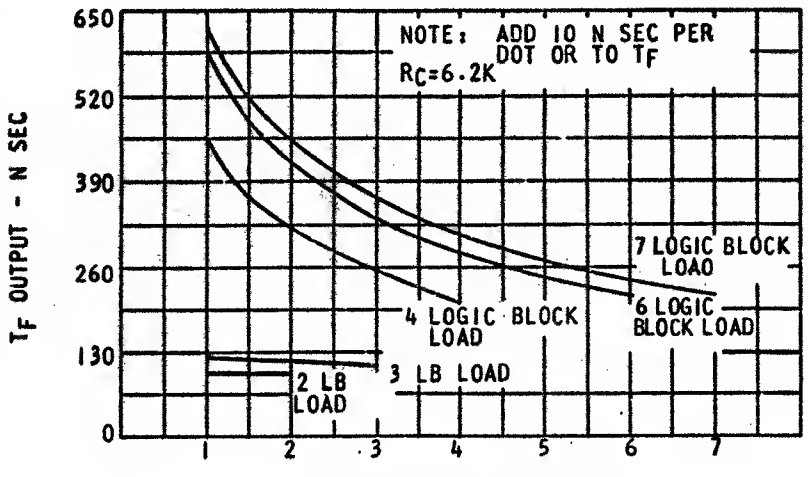
HIGH SPEED SINGLE LEVEL LOGIC BLOCK

OUTPUT FALL TIME VS LOADING



NUMBER OF LOADS SWITCHED

OUTPUT FALL TIME VS LOADING



NUMBER OF LOAOS SWITCHED

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	OATE
ABC	4-2-62

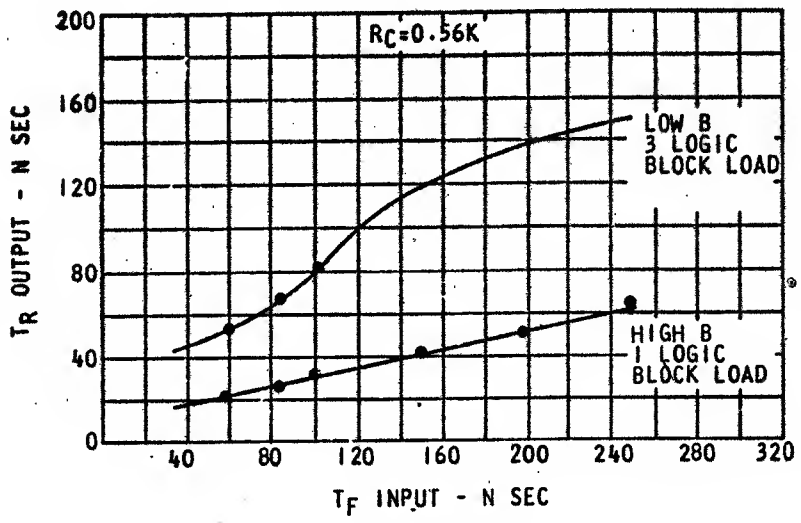
INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHARGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL LOGIC DELAY INFO. - REF DWG			6-19-62	115599					
DESIGN			MODEL							
DETAIL	WH	3-1-62	SCALE							
CHECK	RQ	3-1-62	DRAW							
APPRO			CHECK							

729954

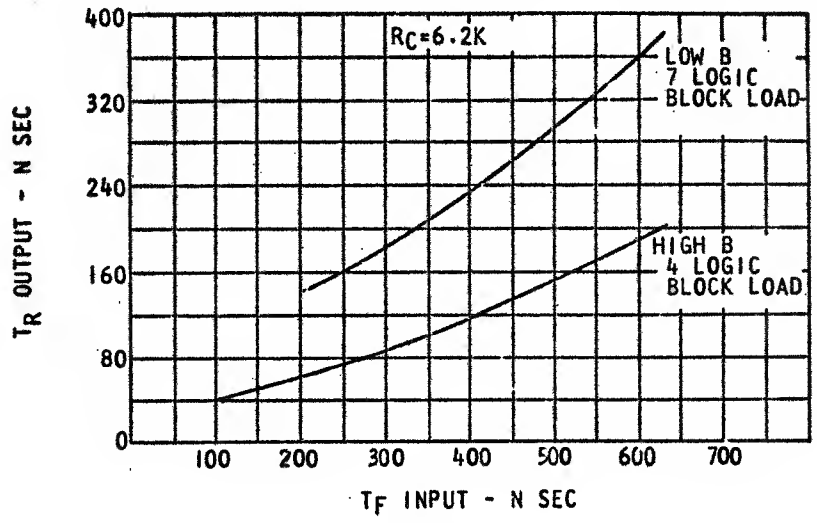
C

LIG 6-4-62

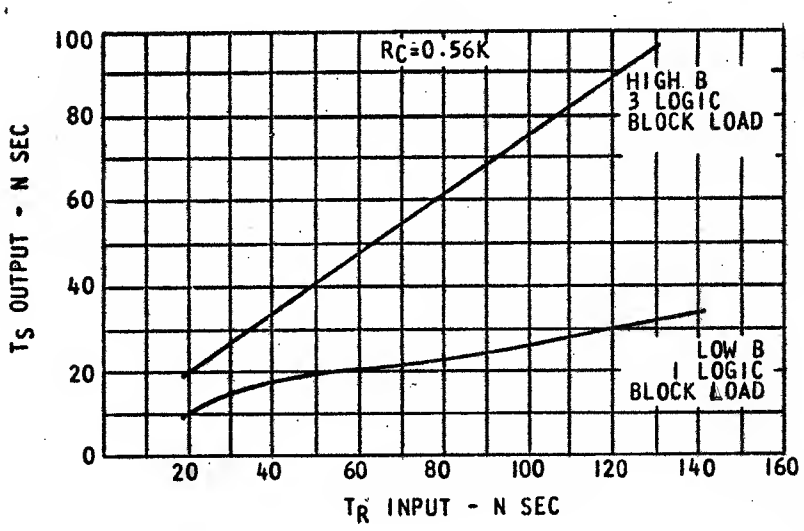
OUTPUT RISE TIME VS INPUT FALL TIME



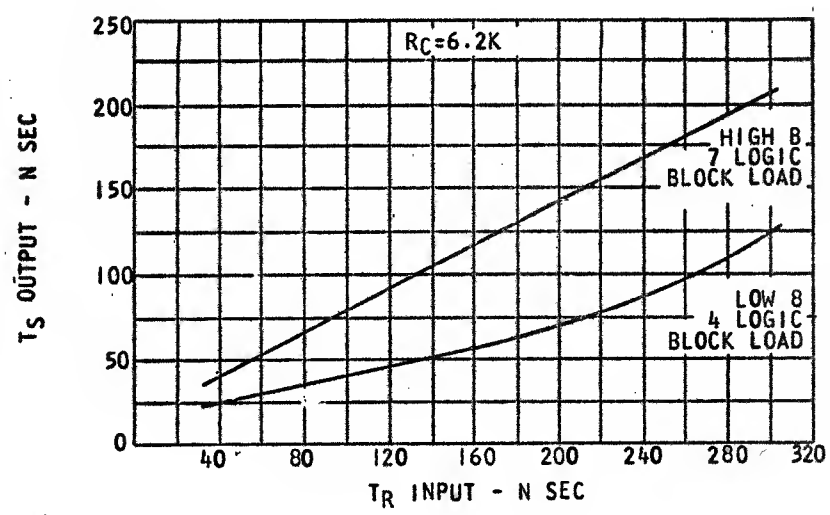
OUTPUT RISE TIME VS INPUT FALL TIME



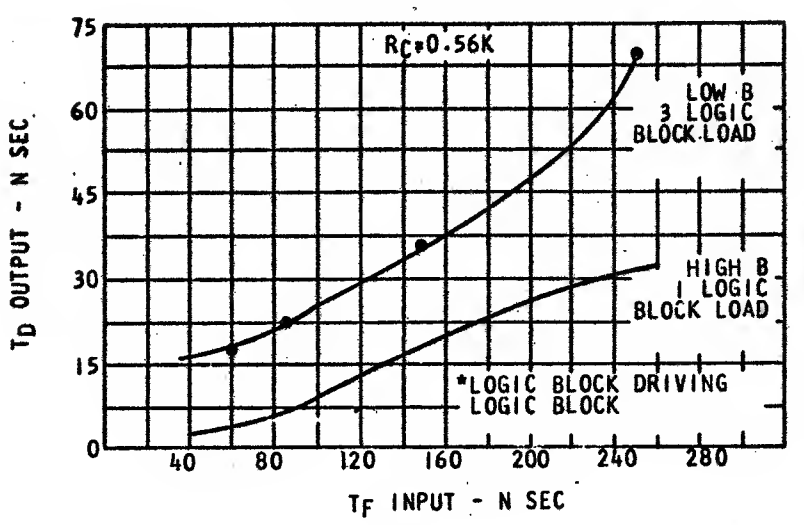
TURN-OFF VS INPUT RISE TIME



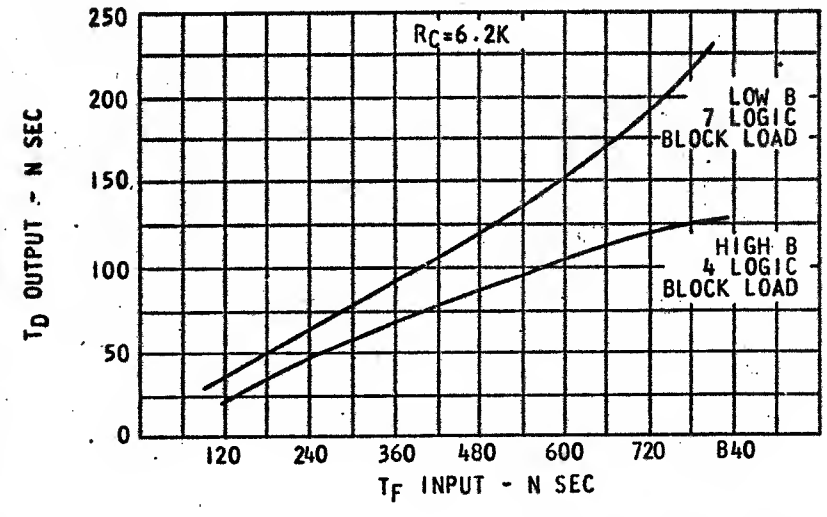
TURN-OFF VS INPUT RISE TIME



TURN-ON VS INPUT FALL TIME*



TURN-ON VS INPUT FALL TIME



CIRCUIT ARD PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

© INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTPL LOGIC DELAY INFO. - REF DWG.				6-29-62	115599					
DESIGN			MODEL								
DETAIL	WH	3-1-62	SCALE								
CHECK	RQ	3-1-62	DRAW								
APPRO			CHECK								

729954

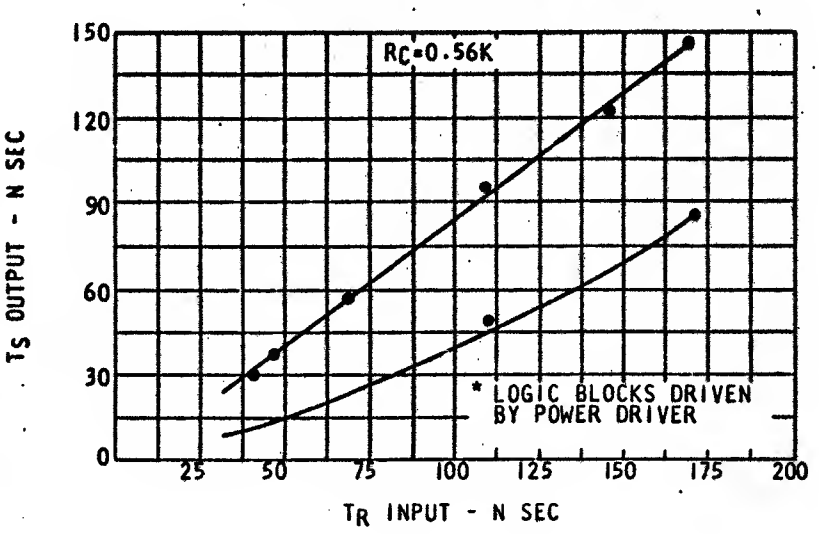
C

LIG 6-4-62

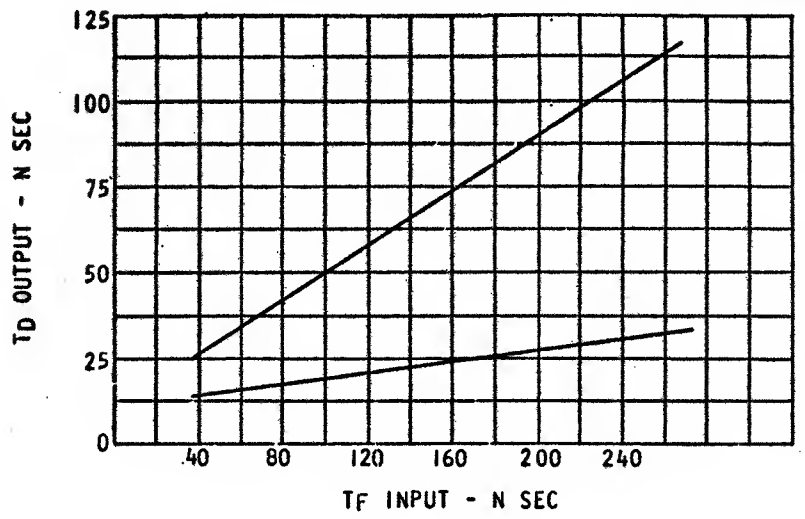
STANDARDS CODE 729954

CARD CODE 729954

TURN-OFF VS RISE TIME INPUT*



TURN-ON VS FALL TIME INPUT (LOGIC BLOCK DRIVEN BY POWER DRIVERS)



C

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

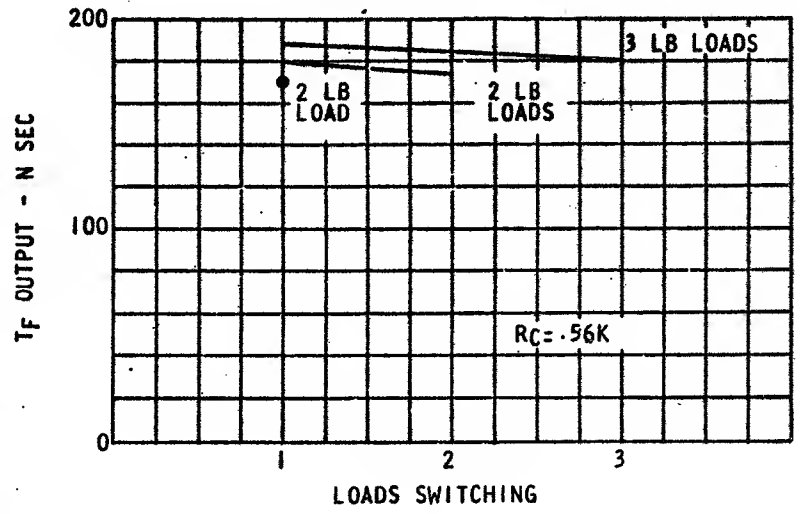
INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL LOGIC DELAY INFO. - REF. DWG.				6-29-62	115599					
DESIGN			MODEL								
DETAIL	WH	3-1-62	SCALE								
CHECK	RQ	3-1-62	DRAW								
APPRO			CHECK								

729954

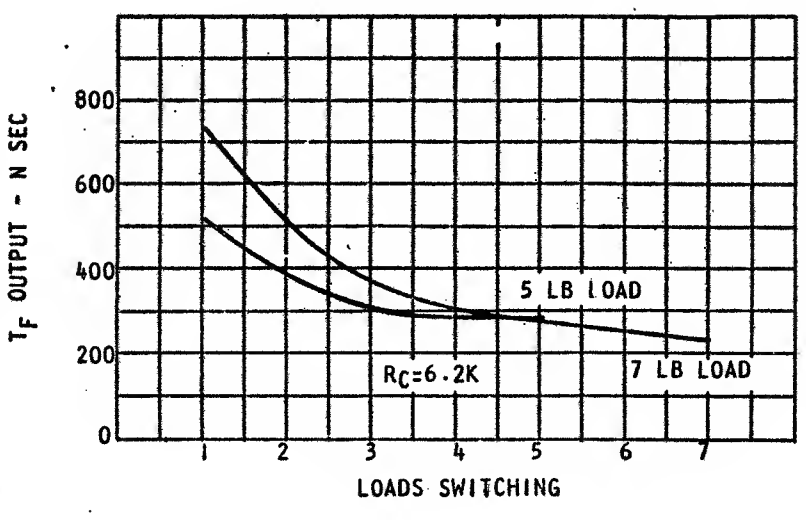
LIG 6-4-62

LOW SPEED SINGLE LEVEL LOGIC BLOCKS

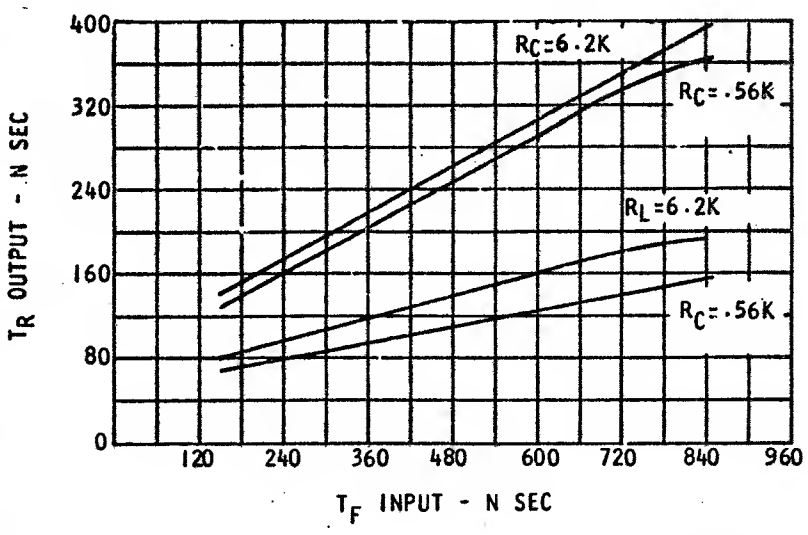
FALL TIME VS LOADING



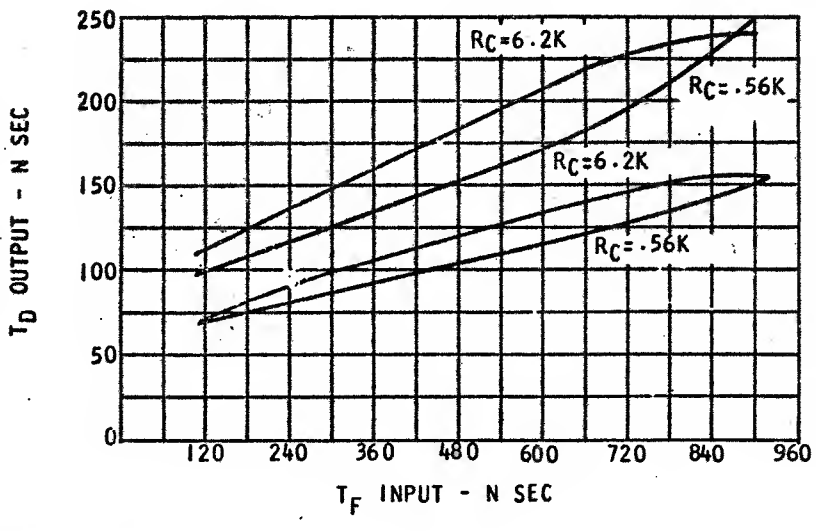
FALL TIME VS LOADING



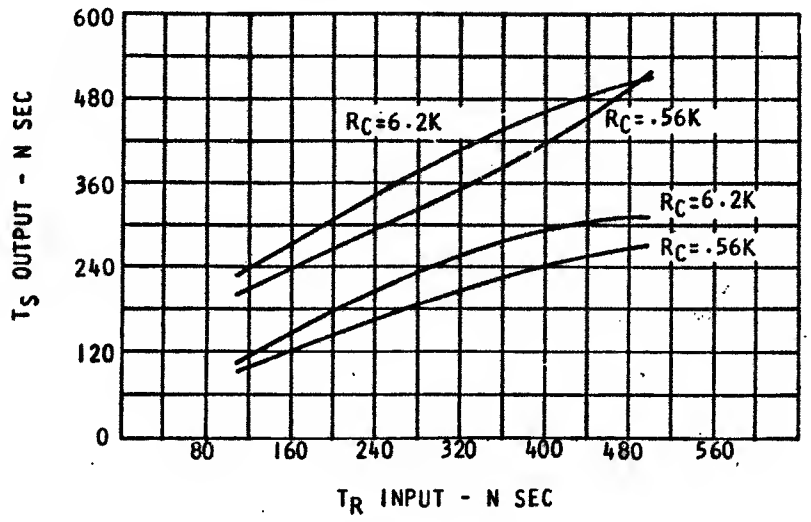
OUTPUT RISE TIME VS INPUT FALL TIME



TURN-OFF VS INPUT FALL TIME



TURN-OFF VS INPUT RISE TIME



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMEGT NO.	729954
NAME	SDTDL LOGIC DELAY				-62	115599						
	INFO. - REF DWG											
DESIGN			MODEL									
DETAIL	WH	3-1-62	SCALE									
CHECK	RQ	3-1-62	DRAW									
APPRO			CHECK									

C

LIG 6-4-62

2-2

STANDARDS CODE

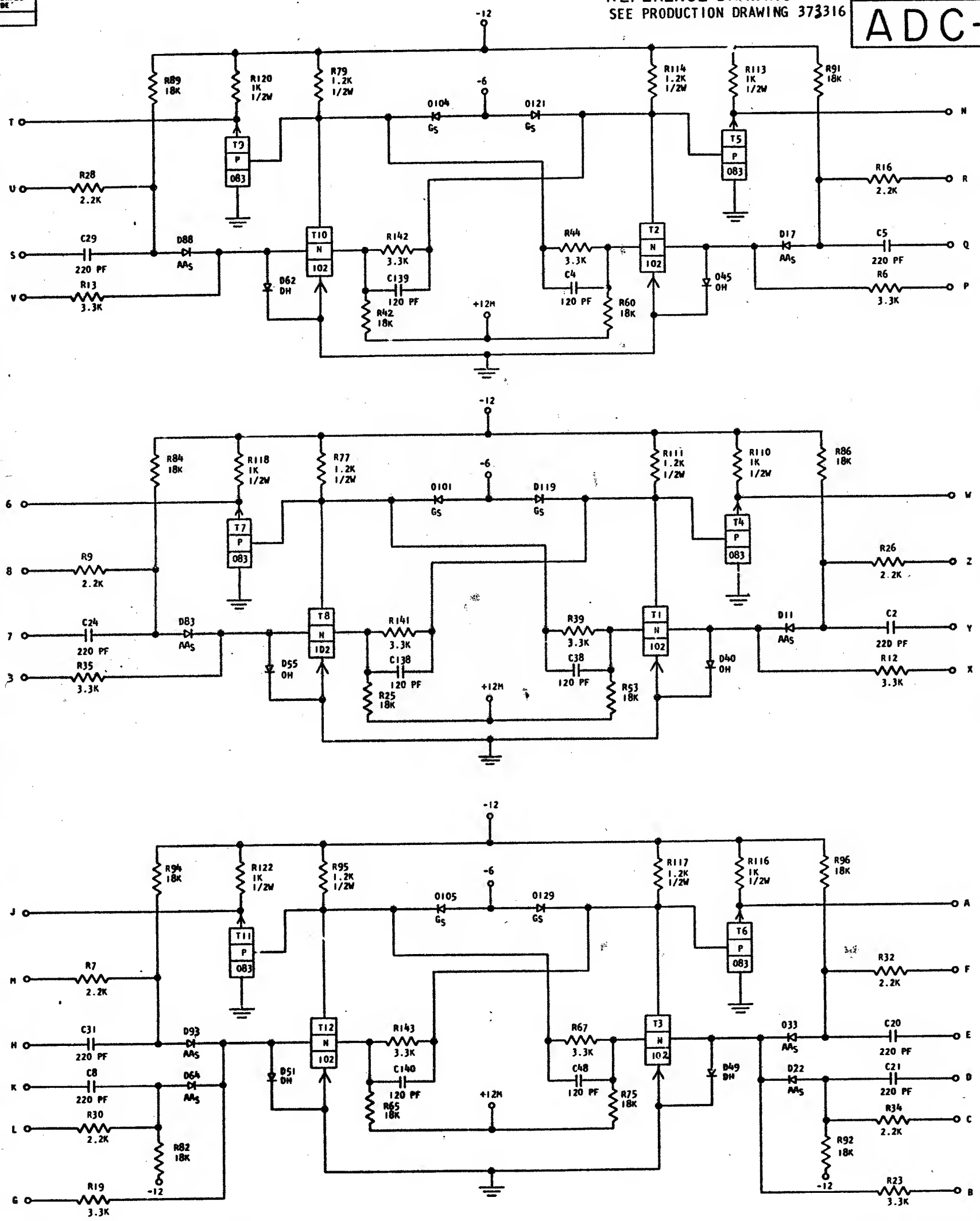
736615

SHEET 1 OF 3

REFERENCE DRAWING
SEE PRODUCTION DRAWING 373316

CARD CODE 736615

ADC-



-12 -6

C1 0.01 UF C102 0.01 UF

VOLTAGE	PIN
GND	1
-6	2
-12	4
+12M	5

CIRCUIT AND PACAAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	LOW SPEED POWER TRIGGER				4-10-63	115643H						736615
DESIGN			MODEL	SMS 1440							736615	
DETAIL			SCALE	NONE								
CHECK			DRAW									
APPRO			CHECK									

C

2-2

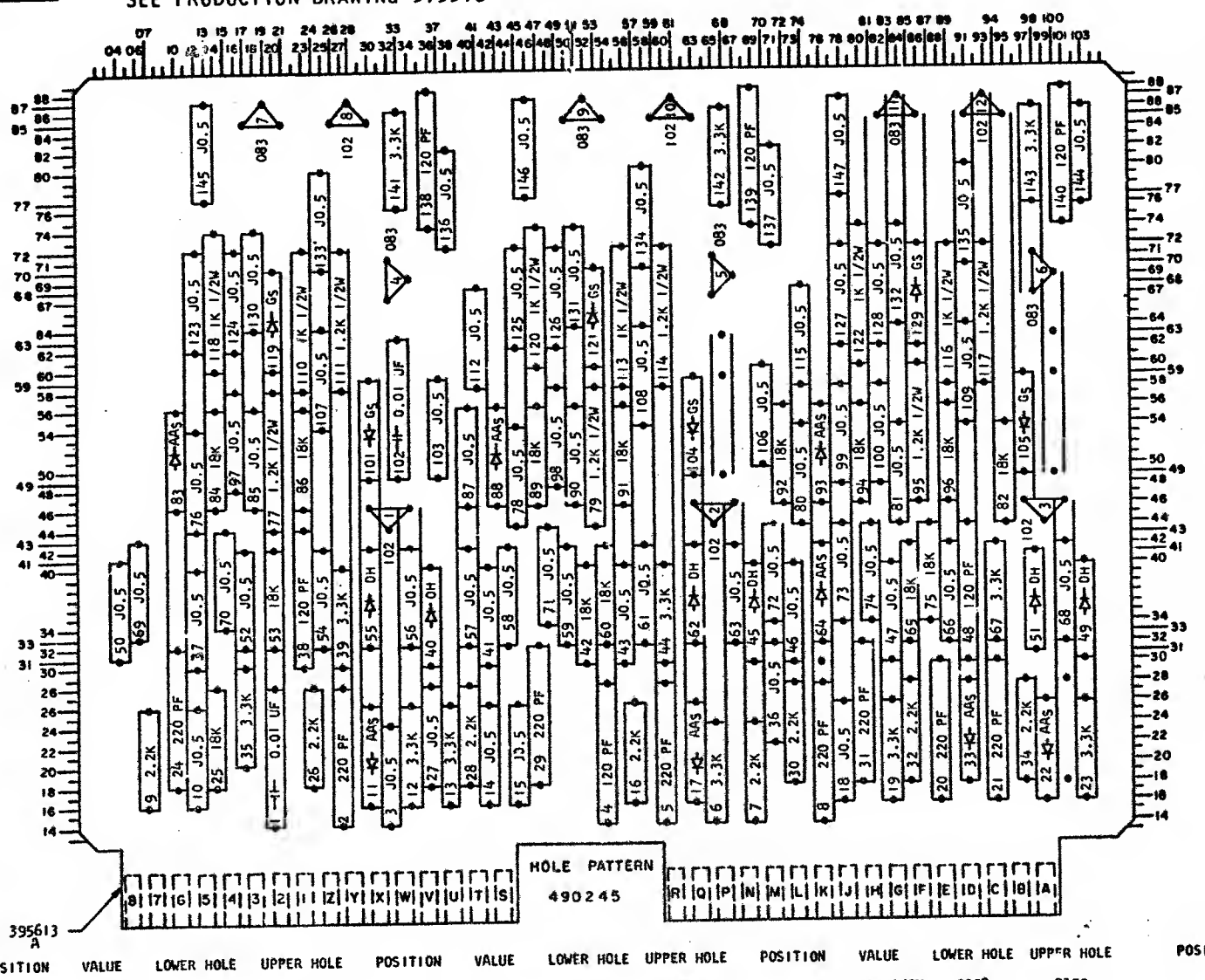
STANDARDS CODE
736615

SHEET 2 OF 3

REFERENCE DRAWING
SEE PRODUCTION DRAWING 373316

CARD CODE	736615
A D C -	

PART NO.	VALUE	QTY.
213693	1K 1/2W	6
216453	2.2K	8
216456	3.3K	12
216474	18K	14
317276	1.2K 1/2W	6
350430	120 PF	6
350436	220 PF	8
369217	OH	6
491008	AAS	8
491228	0.01 UF	2
503592	GS	6
318325	083	6
369179	102	6



POSITION	VALUE	LOWER HOLE	UPPER HOLE
1	0.01 UF	2014	2028
2	220 PF	2714	2728
3	J0.5	3214	3224
4	120 PF	5414	5428
5	220 PF	6014	6028
6	3.3K	6514	6524
7	2.2K	6914	6924
8	220 PF	7614	7628
9	2.2K	0716	0726
10	J0.5	1216	1226
11	AAS	3016	3026
12	3.3K	3416	3426
13	3.3K	3816	3826
14	J0.5	4216	4226
15	J0.5	4516	4526
16	2.2K	5716	5726
17	AAS	6316	6326
18	J0.5	7816	7826
19	3.3K	8316	8326
20	220 PF	8816	8830
21	220 PF	9416	9430
22	AAS	9916	9926
23	3.3K	10316	10326
24	220 PF	1018	1032
25	18K	1418	1428
26	2.2K	2418	2428
27	J0.5	3618	3628
28	2.2K	4018	4028
29	220 PF	4718	4732
30	2.2K	7318	7328
31	220 PF	8018	8032
32	2.2K	8518	8528
33	AAS	9118	9128
34	2.2K	9718	9728
35	3.3K	1720	1730
36	J0.5	7122	7132
37	J0.5	1230	1240
38	120 PF	2330	2344
39	3.3K	2730	2740
40	OH	3630	3640
41	J0.5	4230	4240
42	18K	5230	5240
43	J0.5	5630	5640
44	3.3K	6030	6040
45	DH	6930	6940
46	J0.5	7330	7340
47	J0.5	8330	8340
48	120 PF	9130	9144
49	DH	10330	10340
50	J0.5	0431	0441
51	OH	9831	9841
52	J0.5	1732	1742
53	18K	2032	2042
54	J0.5	2532	2542
55	OH	3032	3042
56	J0.5	3432	3442
57	J0.5	4032	4042
58	J0.5	4432	4442
59	J0.5	5032	5042
60	18K	5432	5442
61	J0.5	5832	5842
62	OH	6332	6342
63	J0.5	6732	6742
64	AAS	7632	7642
65	18K	8532	8542
66	J0.5	8932	8942
67	3.3K	9432	9442
68	J0.5	10132	10142
69	J0.5	0633	0643
70	J0.5	1534	1544
71	J0.5	4834	4844
72	J0.5	7134	7144
73	J0.5	7834	7844
74	J0.5	8134	8144
75	18K	8734	8744
76	J0.5	1244	1254
77	1.2K 1/2W	2044	2058
78	J0.5	4544	4554
79	1.2K 1/2W	5344	5358
80	J0.5	7444	7454
81	J0.5	8444	8454
82	18K	9544	9554
83	AAS	1046	1056
84	18K	1446	1456
85	J0.5	1846	1856
86	18K	2346	2356
87	J0 5	4046	4056
88	AAS	4346	4356
89	18K	4746	4756
90	J0.5	5146	5156
91	18K	5646	5656
92	18K	7246	7256
93	AAS	7646	7656
94	18K	8046	8056
95	1.2K 1/2W	8646	8660
96	18K	8946	8956
97	J0.5	1648	1658
98	J0.5	4948	4958
99	J0.5	7848	7858
100	J0.5	8248	8258
101	GS	3049	3059
102	0.01 UF	3349	3363
103	J0.5	3749	3759
104	GS	6349	6359
105	GS	9749	9759
106	J0.5	7050	7060
107	J0.5	2554	2564
108	J0.5	5854	5864
109	J0.5	9154	9164
110	1K 1/2W	2358	2372
111	1.2K 1/2W	2758	2772
112	J0.5	4158	4168
113	1K 1/2W	5658	5672
114	1.2K 1/2W	6058	6072
115	J0.5	7458	7468
116	1K 1/2W	8958	8972
117	1.2K 1/2W	9358	9372
118	1K 1/2W	1460	1474
119	GS	2060	2070
120	1K 1/2W	4760	4774
121	GS	5360	5370
122	1K 1/2W	8060	8074
123	J0.5	1262	1272
124	J0.5	1662	1672
125	J0.5	4562	4572
126	J0.5	4962	4972
127	J0.5	7862	7872
128	J0.5	8262	8272
129	GS	8662	8672
130	J0.5	1864	1874
131	J0.5	5164	5174
132	J0.5	8464	8474
133	J0.5	2570	2580
134	J0.5	5870	5880
135	J0.5	9170	9180
136	J0.5	3872	3882
137	J0.5	7172	7182
138	120 PF	3674	3688
139	120 PF	6974	6988
140	120 PF	10174	10188
141	3.3K	3376	3386
142	3.3K	6676	6686
143	3.3K	9876	9886
144	J0.5	10376	10386
145	J0.5	1377	1387
146	J0.5	4677	4687
147	J0.5	7877	7887

POSITION	TYPE	E	B	C
1	102	3046	3244	3446
2	102	6346	6544	6746
3	102	9746	9944	10146
4	083	3267	3469	3271
5	083	6567	6769	6571
6	083	9867	10069	9871
7	083	2185	1987	1785
8	102	3085	2887	2685
9	083	5485	5287	5085
10	102	6385	6187	5985
11	083	8685	8487	8285
12	102	9585	9387	9185

CIRCUIT ARD PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.													
NAME	LOW SPEED POWER TRIGGER				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	736615
					4-10-63	115643H						
DESIGN			MODEL	SMS 1440							736615	
DETAIL			SCALE	NONE								
CHECK			DRAW									
APPRD			CHECK									

C

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736615

736615

ADC–

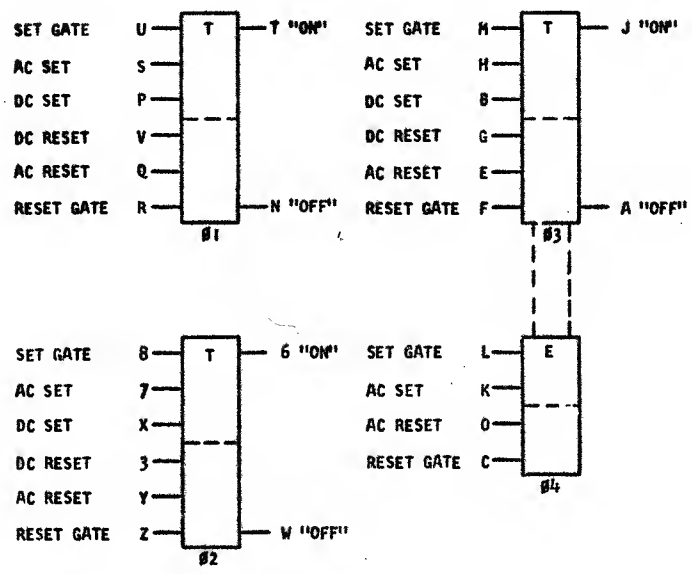
P/N: 373316 EC: Ø113568

SHEET 3 OF 3

REFERENCE DRAWING
PRODUCTION DRAWING 373316

SHEET 3 OF 3

LOW SPEED POWER TRIGGER



SEQUENCE OF OPERATION

1. WHEN THE TRIGGER IS SET, THE "ON" OUTPUT IS AT -6V AND THE "OFF" OUTPUT IS ØV.
2. WHEN THE TRIGGER IS IN A RESET CONDITION THE "ON" OUTPUT IS AT ØV AND THE "OFF" OUTPUT IS AT -6V.
3. TRIGGER IS SET BY
   A.) A NEGATIVE VOLTAGE LEVEL APPLIED TO THE DC SET INPUT OR
   B.) AN UP LEVEL AT THE SET GATE INPUT IN CONJUCTION WITH A POSITIVE SHIFT AT THE AC SET INPUT.
4. TRIGGER IS RESET BY
   A.) A NEGATIVE VOLTAGE LEVEL AT THE DC RESET INPUT OR
   B.) AN UP LEVEL AT THE RESET GATE INPUT IN CONJUNCTION WITH A POSITIVE SHIFT AT THE AC RESET INPUT.

NOTES:

1. THE GATES MUST BE AT THE UP LEVEL 150NS BEFORE THE AC SET ARRIVES.
2. THE AC SET SHOULD BE AT LEAST 70NS WIDE AND ITS RISE TIME 70NS OR LESS.
3. TRIGGER MAY BE USED IN A BINARY STATE IF BOTH AC INPUTS ARE COMMON.
4. THE NON-INVERTING POWER DRIVER CONNECTED IN EACH CIRCUIT IS USED TO DRIVE LARGE LOGIC BLOCKS.

PINS	SIGNAL NAME		WAVESHAPE	LEVELS	MIN	MAX
U,L 8,H	Y	SET GATE		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
S,K 7,H	Y	AC SET		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
P X,B	Y	DC SET		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
V 3,G	Y	DC RESET		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
Q,D Y,E	Y	AC RESET		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
R,C Z,F	Y	RESET GATE		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
T 6,J	Y	"ON" OUTPUT		UP	-1.10V	-.22V
				DOWN	-5.83V	-7.3V
N W,A	Y	"OFF" OUTPUT		UP	-1.10V	-.22V
				DOWN	-5.83V	-7.3V

DELAY - NSEC

	TON MAX	TON MIN	TRISE MAX	TRISE MIN	TOFF MAX	TOFF MIN	TFALL MAX	TFALL MIN
BINARY OPERATION:	360	46	50	25	845	180	635	155
GATED:	370	41	50	20	700	130	475	110

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	LOW SPEED POWER TRIGGER				4-10-63	115643H					
DESIGN			MODEL	SMS 1440							736615
DETAIL			SCALE	NONE							
CHECK			DRAW	MDE 1-25-63							
APPRO			CHECK								

736615

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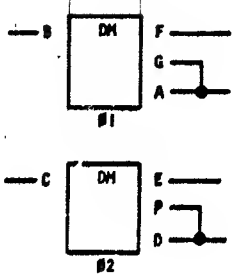
734383

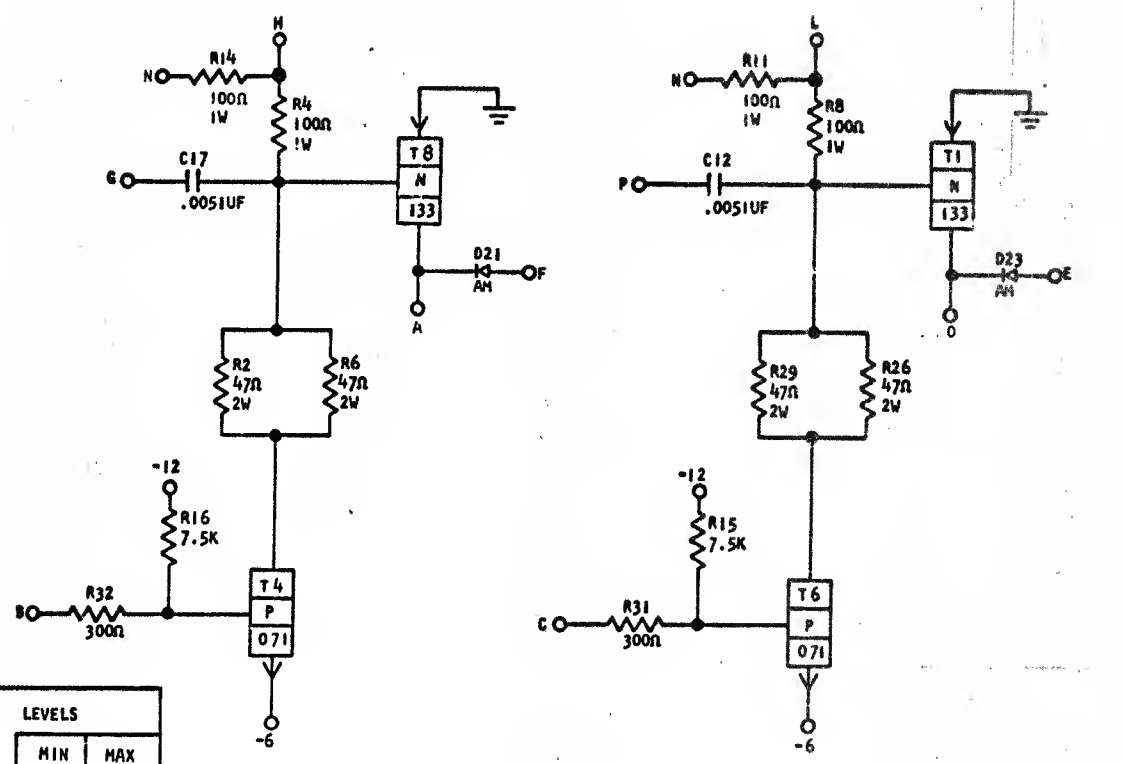
ADF—

P/N: 372375

REFERENCE DRAWING
PRODUCTION DRAWING 372375

DAP - SOLENOID DRIVER



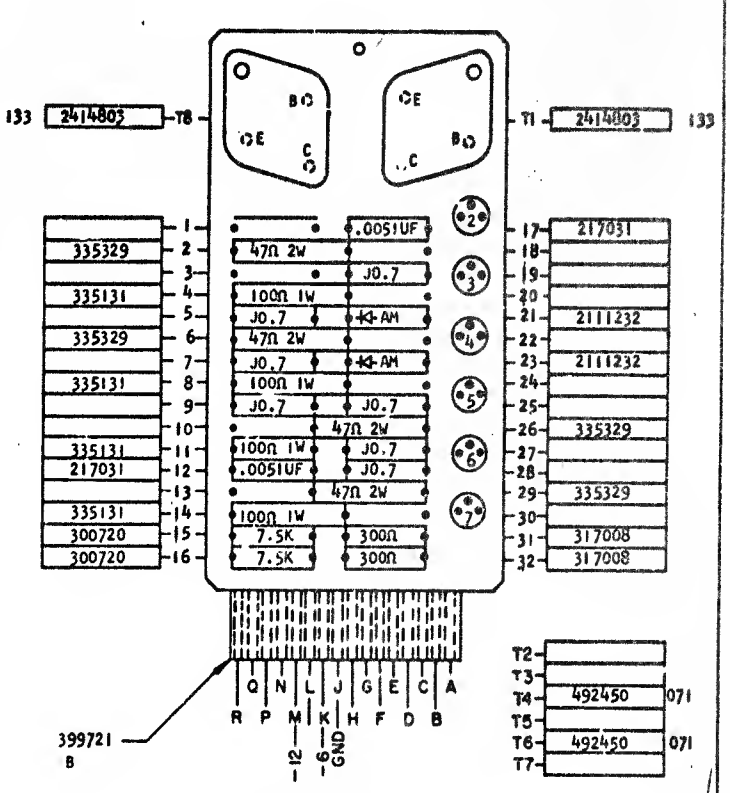


SEQUENCE OF OPERATION

1. INPUT UP: TRANSISTORS ON, OUTPUT UP.
2. INPUT DOWN: TRANSISTORS OFF, OUTPUT DOWN.

PINS	SIGNAL NAME		WAVESHAPE	LEVELS	MIN	MAX
B, C	Y	INPUT		UP	-0.65V	-.05V
				DOWN	-5.81V	-12V
A, D	V	OUTPUT		UP	-.8V	±.24W
				DOWN	---	---*
F, E		CLAMP		UP	-12V	-12V
				DOWN	-12V	-12V

* THE DOWN LEVEL DEPENDS ON THE LOAD RETURN VOLTAGE



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.													
NAME	DAP - SOLENOID DRIVER						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
							4-17-63	116800A					
DESIGN			MODEL				6-17-63	117811					
DETAIL			SCALE	NONE			5-11-65	123738					
CHECK			DRAW	MDE	2-8-63		18DEC67	D132189					
APPRO	[illegible]	4-17-63	CHECK										

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734383

729902

STANDARDS CODE

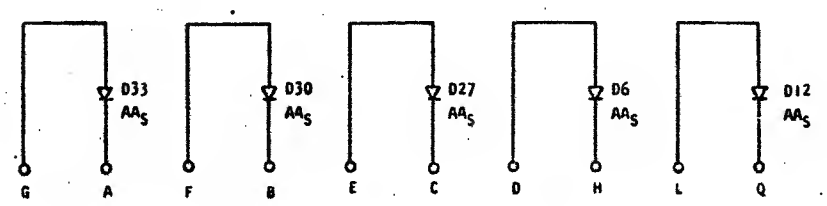
CARD CODE 729902

A J T -

REFERENCE DRAWING

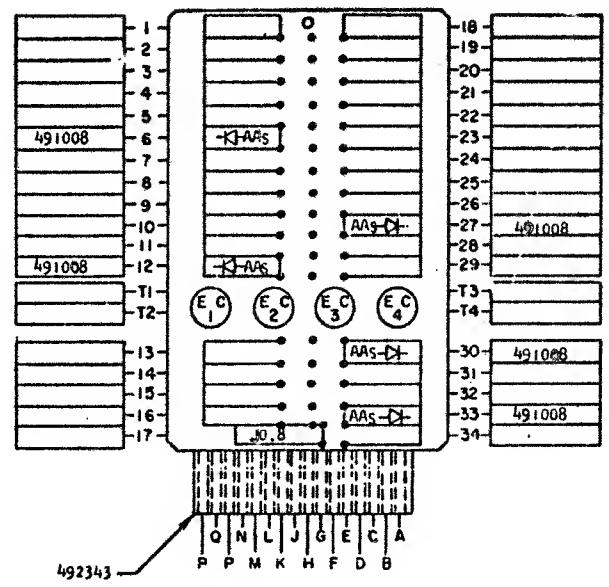
SEE PRODUCTION DRAWING 370564

ALLOY-DIODES, TYPE AA_S



APPLICATION NOTES

THESE DIODES CAN BE USED AS INPUTS TO EITHER P OR N TYPE LOGIC BLOCKS DEPENDING ON HOW THE PINS ARE CONNECTED.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME CARD ASM TSTR - ALLOY - DIODES, TYPE AAS					6-29-62	115599						729902
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG 3-17-62								
APPRO			CHECK									

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734325

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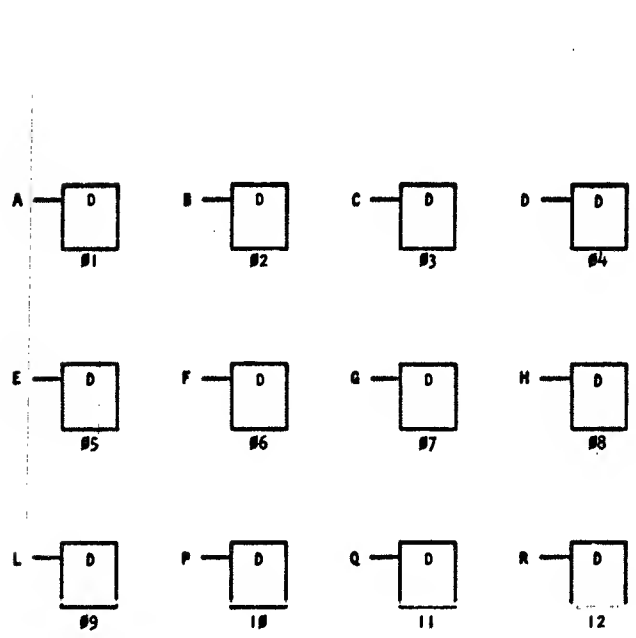
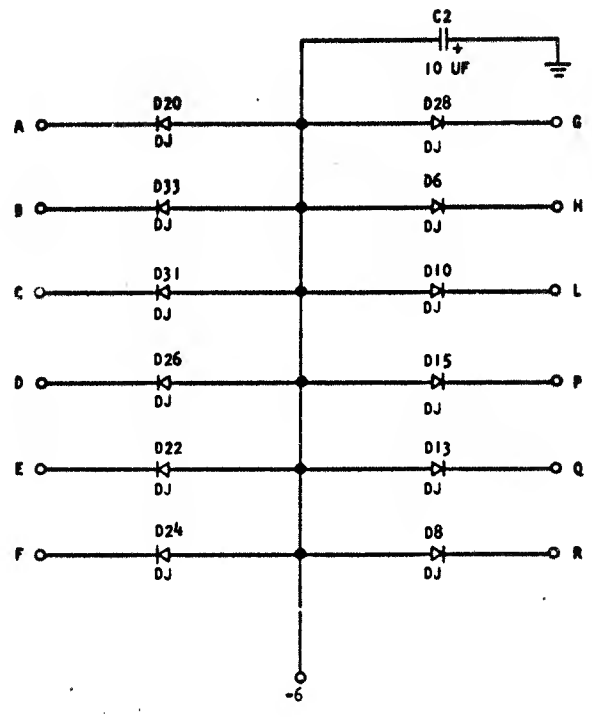
P/N: 370690

REFERENCE DRAWING
PRODUCTION DRAWING 370690

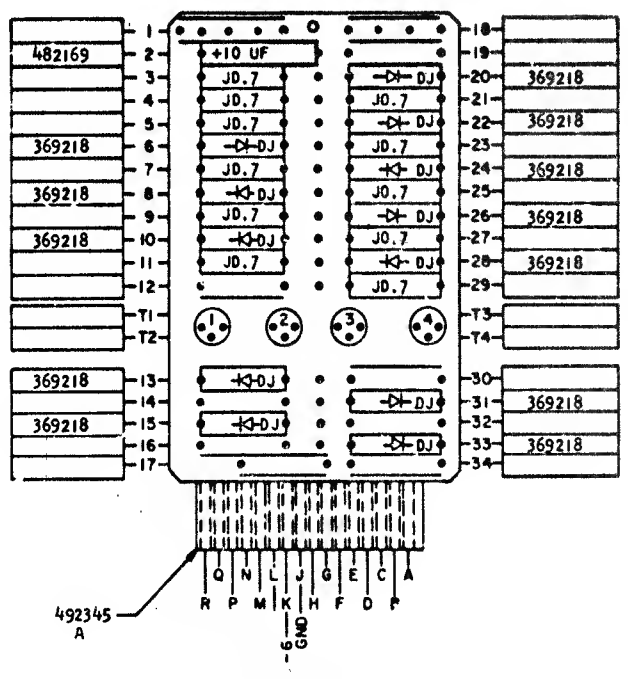
DJ DIODE CARD





OTHER DESIGNATIONS:

D-6



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.														
NAME DJ DIODE CARD						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734325
						3-25-63	116800						
						12OCT65	125834						
DESIGN			MODEL	SMS 1440									
DETAIL			SCALE	NONE									
CHECK			DRAW	MDE 12-19-62									
APPRD		3-25-63	CHECK										

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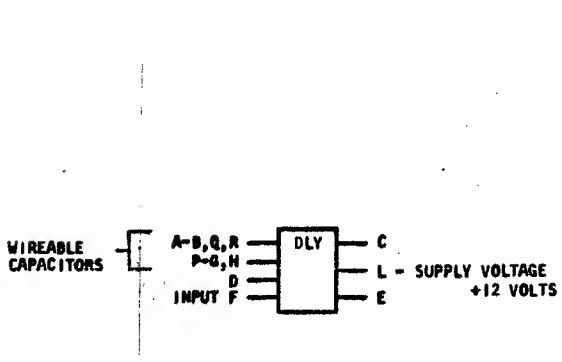
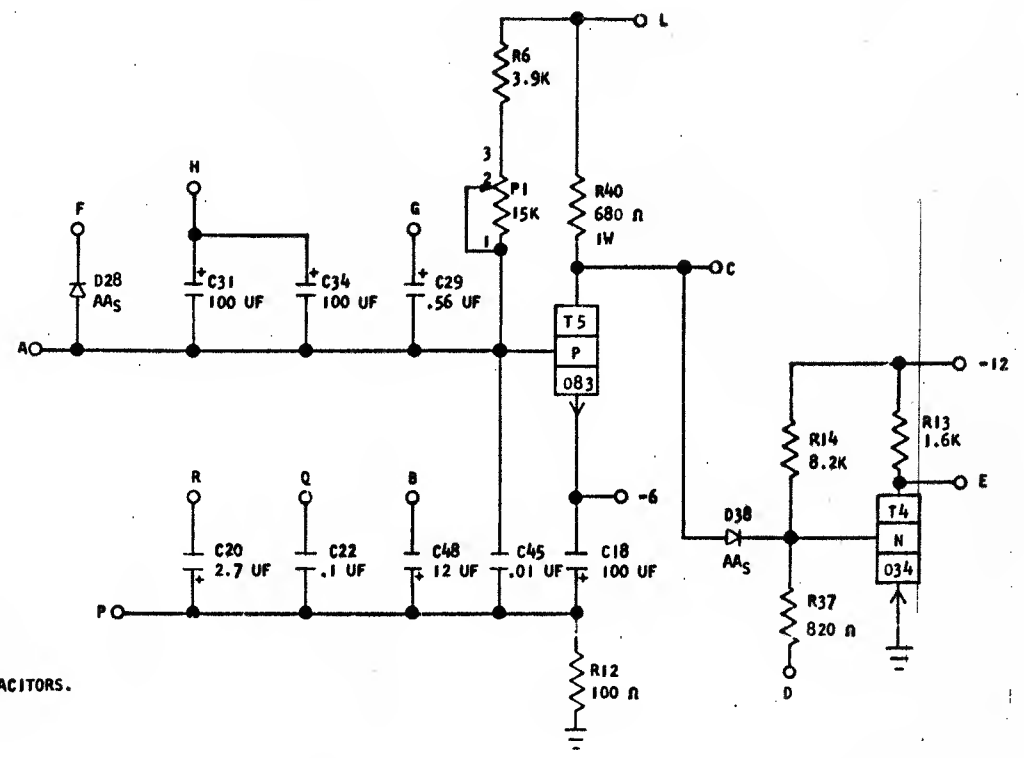
AQQ—

P/N: 370703

REFERENCE DRAWING
PRODUCTION DRAWING 370703

GENERAL DELAY CIRCUIT





SEQUENCE OF OPERATION

1. INPUT LEVEL DOWN, OUTPUT C UP, OUTPUT E DOWN.
2. INPUT SWITCHING TO UP LEVEL, OUTPUT C DELAYED THEN SWITCHES TO DOWN LEVEL. OUTPUT E DELAYED THEN SWITCHES TO UP LEVEL.
3. THE DELAY OF THE POSITIVE EDGE IS DETERMINED BY THE WIREABLE CAPACITORS. THE OUTPUT REMAINS AS LONG AS INPUT REMAINS UP.

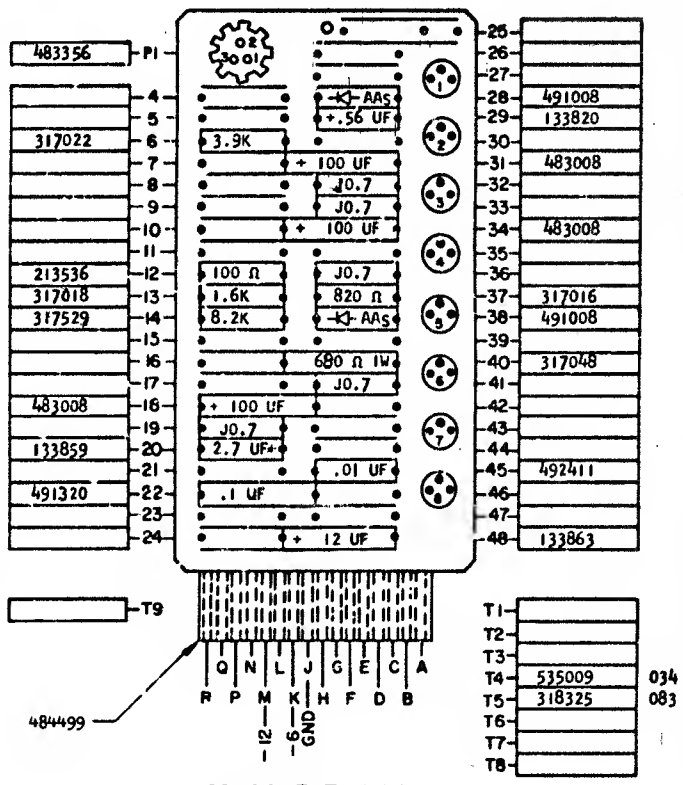
NOTE: PIN D GROUNDED

PINS	SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
F	INPUT		UP	-5.31V	+.24V
			DOWN	-6.95V	-12.48V
E	OUTPUT		UP	-.54V	+.24V
			DOWN	-5.81V	-12.48V
C	OUTPUT		UP	+1.44V	+6.7V
			DOWN	-4.47V	-6.24V

DELAY*

	POT SET AT OK	POT SET AT 15K
INPUT F	7 USEC	34 USEC
A-Q	72 USEC	370 USEC
P-G	300 USEC	1.75 MSEC
A-R	1.80 MSEC	9 MSEC
A-B	9 MSEC	39 MSEC
P-H	140 MSEC	650 MSEC

* DELAY IS MEASURED FROM THE TIME D28 REVERSE BIASES TO WHEN OUTPUT C CROSSES GROUND.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPRDVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	GENERAL DELAY CIRCUIT					4-25-63	1168008					
						9-17-63	117832					
DESIGN			MODEL	SMS 1460		7-1-64	119012-B					
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE	1-3-63							
APPRO	RCF	4-25-63	CHECK									

734340

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FORM 88-101

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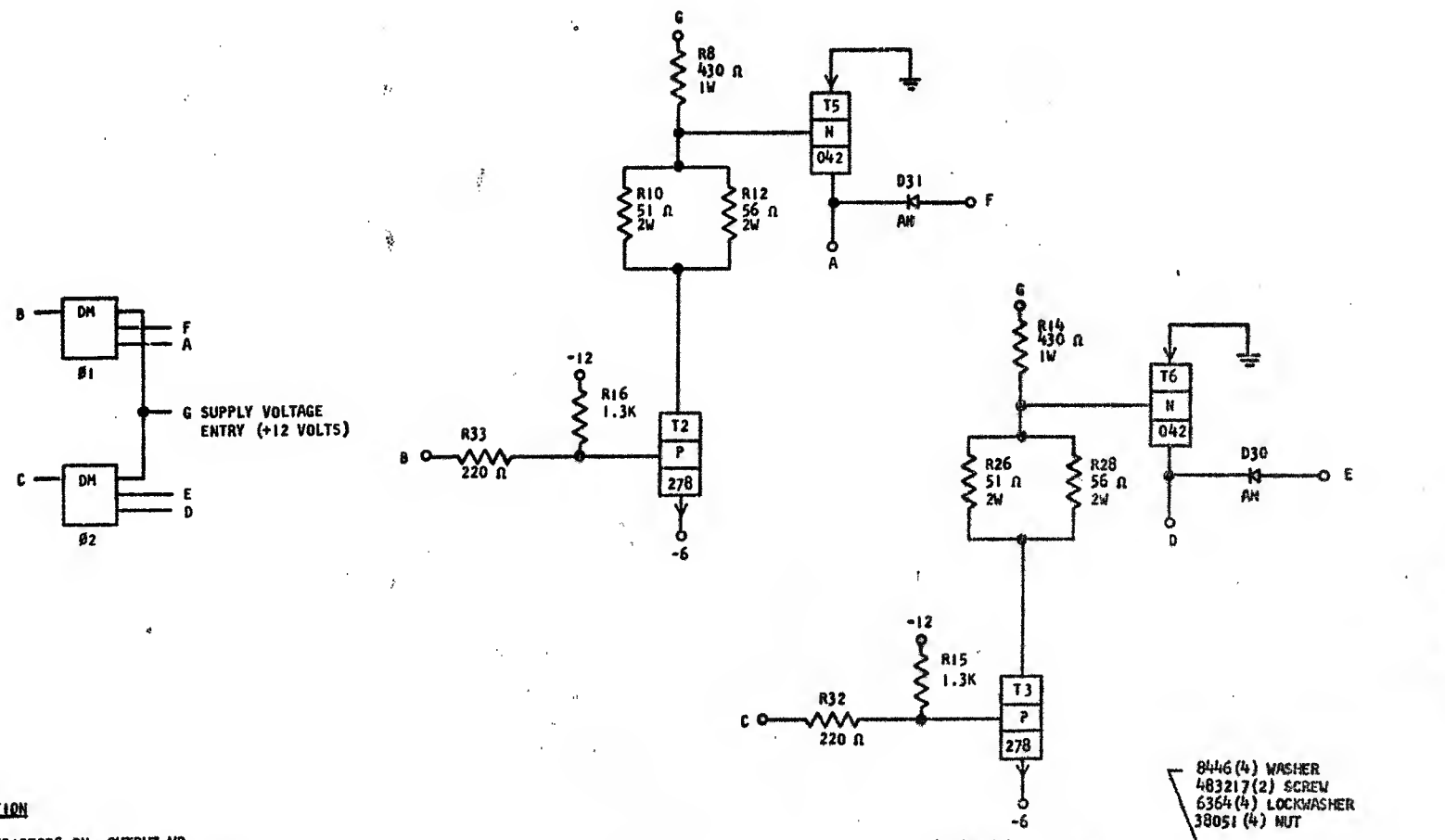
ASQ-

P/N: 372245

REFERENCE DRAWING
PRODUCTION DRAWING 372245

ALLOY CLUTCH MAGNET DRIVER



COMPONENT SIDE

SEQUENCE OF OPERATION

1. INPUT UP: TRANSISTORS ON, OUTPUT UP.
2. INPUT DOWN: TRANSISTORS OFF, OUTPUT DOWN.

PINS	SIGNAL NAME		WAVESHAPE	LEVELS	MIN	MAX
B,C	Y	INPUT		UP	-.65V	-.05V
				DOWN	-5.81V	-12V
A,D	V	OUTPUT		UP	-.8V	+.24V
				DOWN	-18V	-22V
F,E		CLAMP		UP	-12V	-12V
				DOWN	-12V	-12V

DELAY

TURN ON (USEC) 1
TURN OFF (USEC) 30

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	ALLOY CLUTCH MAGNET DRIVER					3-25-63	116800					
						17MAY65	122676	GLK				
DESIGN			MODEL			15JAN68	132410	GWS				
DETAIL			SCALE	NONE								
CHECK			DRAW	MOE	1-3-63							
APPRO		3-25-63	CHECK									

734342

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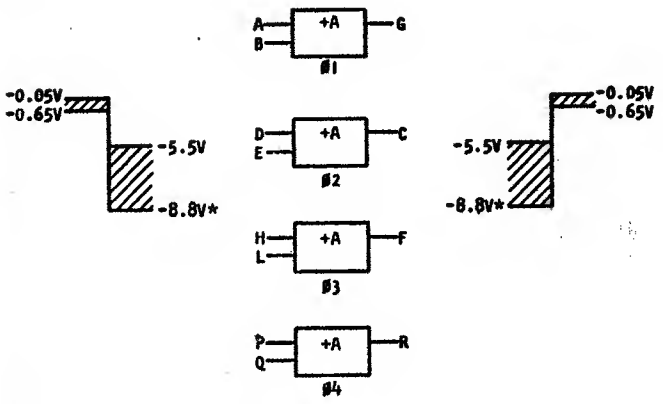
AXA-

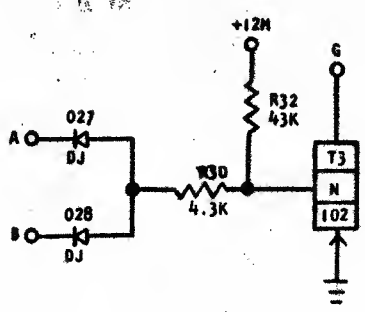
734306

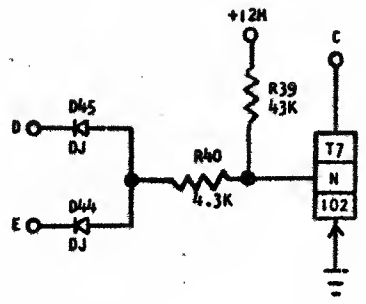
REFERENCE DRAWING
PRODUCTION DRAWING 372197

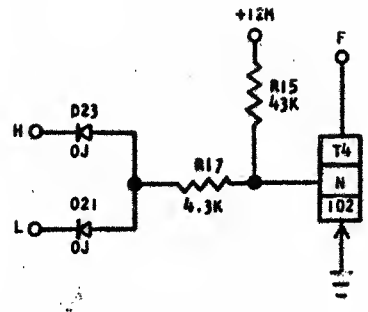
SDTDL LS 4 2-WAY POSITIVE AND LOGIC BLOCKS WITHOUT LOADS

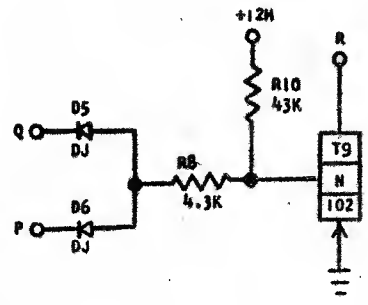


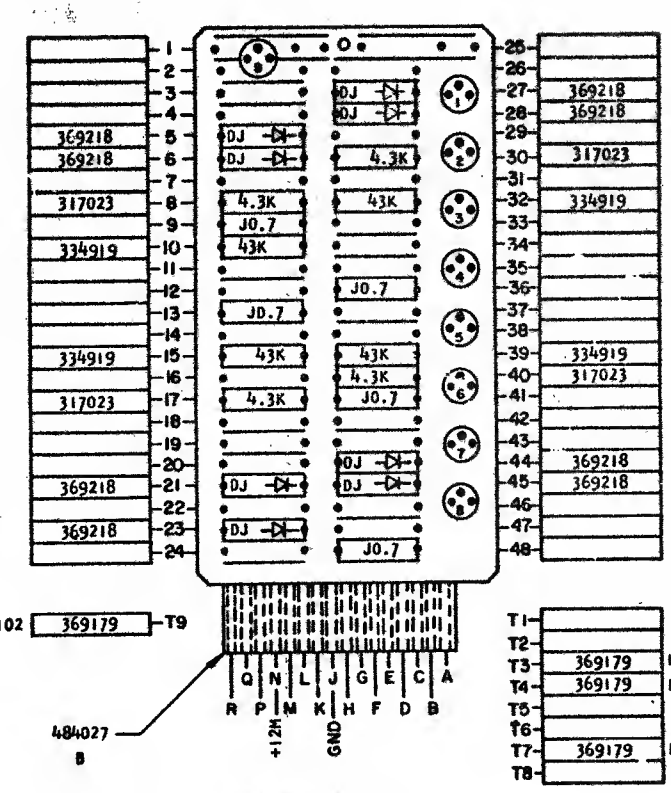
* FUNCTION OF LOAD











OTHER DESIGNATIONS:

-0, +A0, -0A, +AA, -00

SEQUENCE OF OPERATION

1. ALL INPUTS UP: TRANSISTOR OFF, OUTPUT DOWN.
2. ANY INPUT DOWN: TRANSISTOR ON, OUTPUT UP.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
N.A.F.	20FEB62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.	
NAME	SDTDL LS 4 2-WAY POS AND LOGIC BLOCKS WITHOUT LOADS				3-25-63	116800						734306
					10-21-63	118933						
DESIGN			MODEL	SMS	10DEC65	126162	GLK					
DETAIL			SCALE	NONE	23FEB66	127160	GLK					
CHECK			DRAW	HOE 12-10-62								
APPRO	[illegible] 3-25-63		CHECK									

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734309

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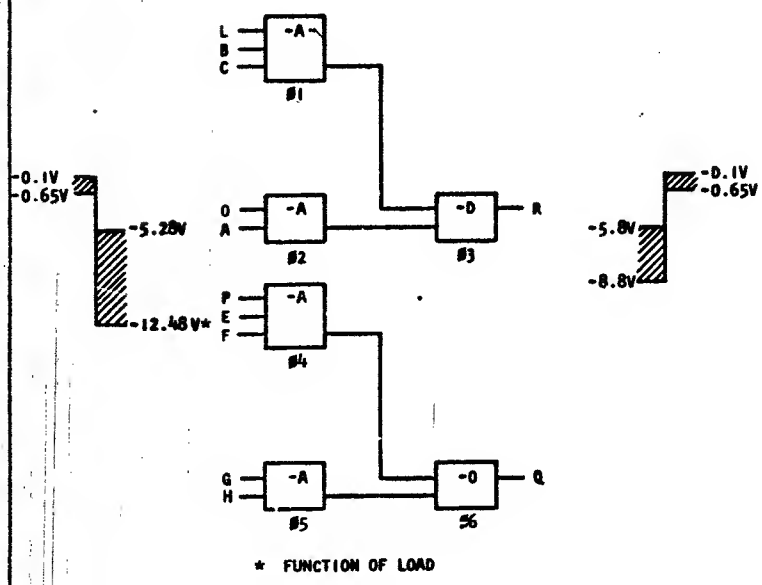
AXC-

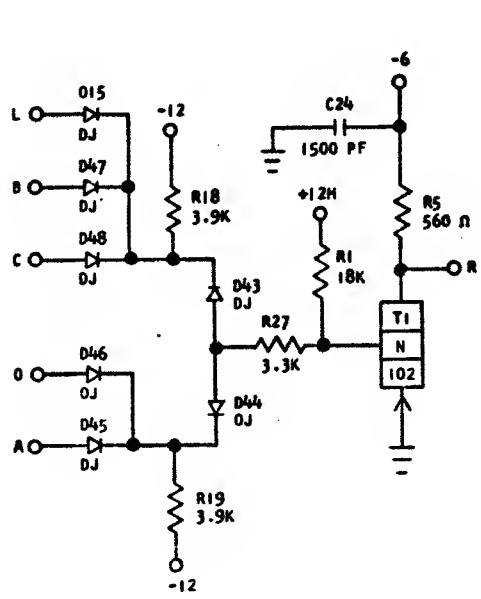
P/N 372202 EC: 0114295

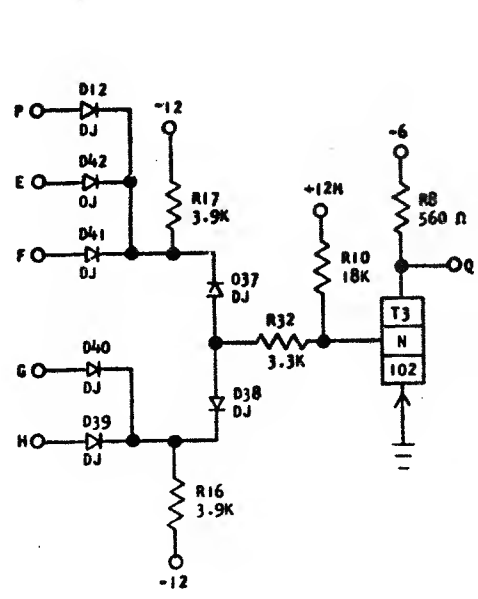
REFERENCE DRAWING
PRODUCTION DRAWING 372202

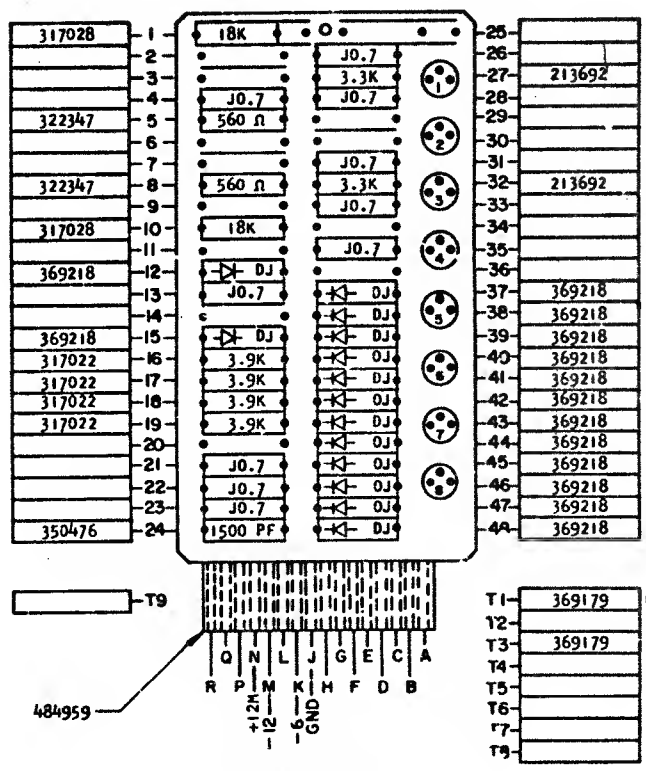
SDTDL LS ONE 2-WAY, ONE 3-WAY NEGATIVE AND-NEGATIVE OR LOGIC BLOCKS WITH LOADS



* FUNCTION OF LOAD







COMPONENT SIDE

OTHER DESIGNATIONS:

CONF. 1,2,4,5 +0
CONF. 3,6 +A,-00,+AA,-0A,+A0

SEQUENCE OF OPERATION

1. PINS L, B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D43.
2. PINS A AND D MUST BE DOWN TO HAVE A DOWN LEVEL AT D44.
3. EITHER DOWN LEVEL AT D43 OR D44 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER L,B OR C UP WILL CAUSE AN UP LEVEL AT D43.
5. EITHER D OR A UP WILL CAUSE AN UP LEVEL AT D44.
6. BOTH LEVELS AT D43 AND D44 MUST BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTOL LS 1 2-WAY, 1 3-WAY NEG AND-NEG OR LOGIC BLOCKS WITH LOADS				3-25-63	116800					
DESIGN			MODEL	SMS 1440							
DETAIL			SCALE	NONE							
CHECK			DRAW	MOE 12-12-62							
APPRO	KES 3-25-63		CHECK								

734309

C

734310

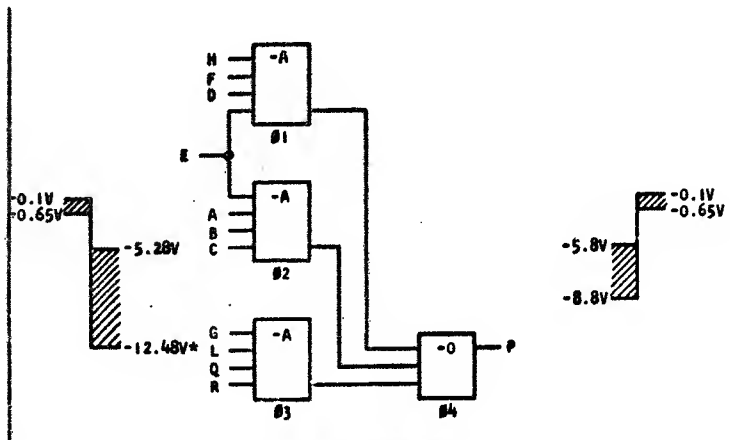
734310

AXG-

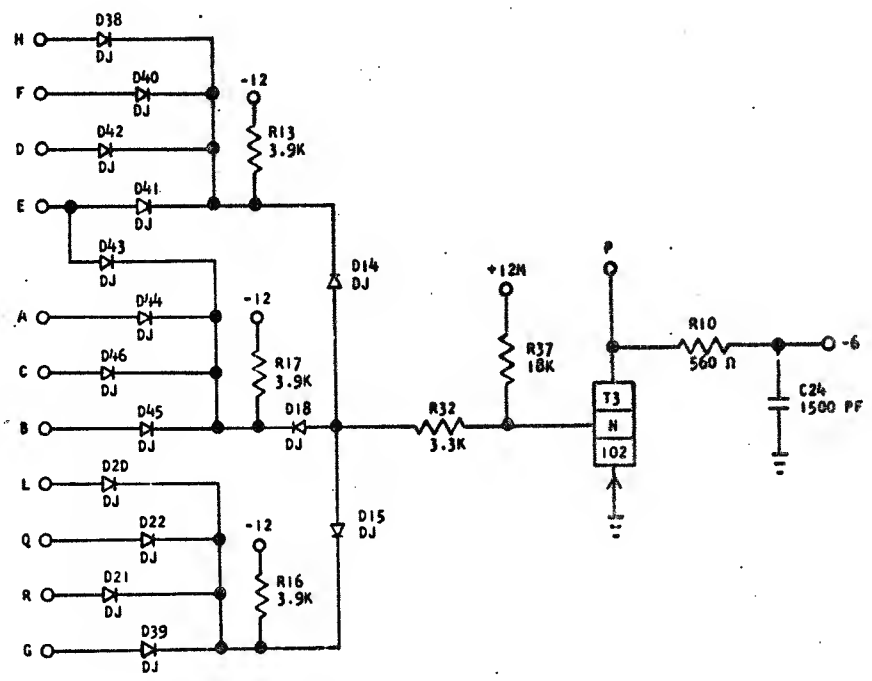
P/N: 372206 EC: 0114295

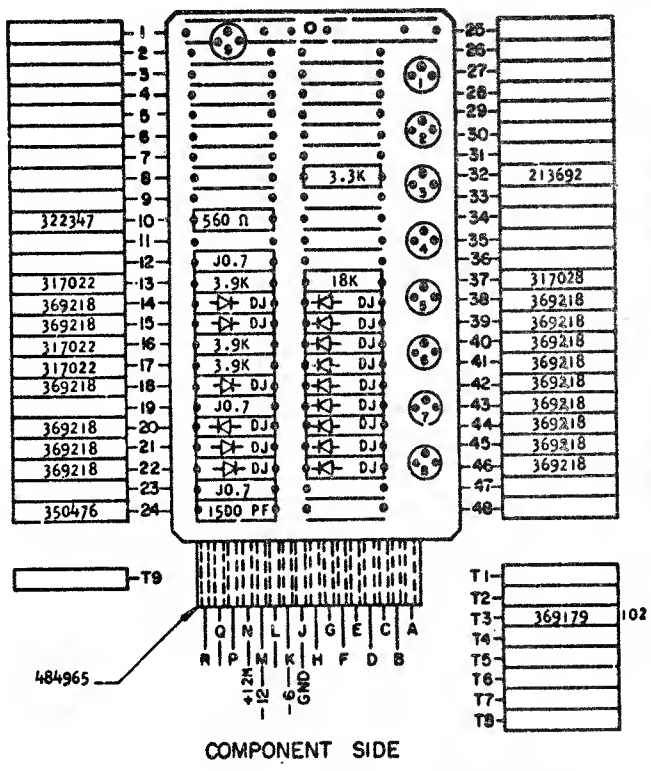
REFERENCE DRAWING
PRODUCTION DRAWING 372206

SDTDL LS THREE 4-WAY NEGATIVE AND-NEGATIVE OR LOGIC BLOCKS WITH LOADS



* FUNCTION OF LOAD





COMPONENT SIDE

OTHER DESIGNATIONS

CONF. 1-3 +0
CONF. 4 +A,-00,+AA,-0A,+A0

SEQUENCE OF OPERATION

1. PINS A,B,C,E MUST BE DOWN TO HAVE A DOWN LEVEL AT D18.
2. PINS G,L,Q,R MUST BE DOWN TO HAVE A DOWN LEVEL AT D15.
3. A DOWN LEVEL AT D14, OR D15, OR D18 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER G,L,Q OR R UP WILL CAUSE AN UP LEVEL AT D15.
5. EITHER A,B,C OR E UP WILL CAUSE AN UP LEVEL AT D18.
6. THE LEVELS AT D18,D15 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	SDTDL LS 3 4-WAY NEG AND-NEG OR LOGIC BLOCKS WITH LOADS				3-25-63	116800						734310
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE 12-12-62								
APPRO	[illegible]	3-25-63	CHECK									

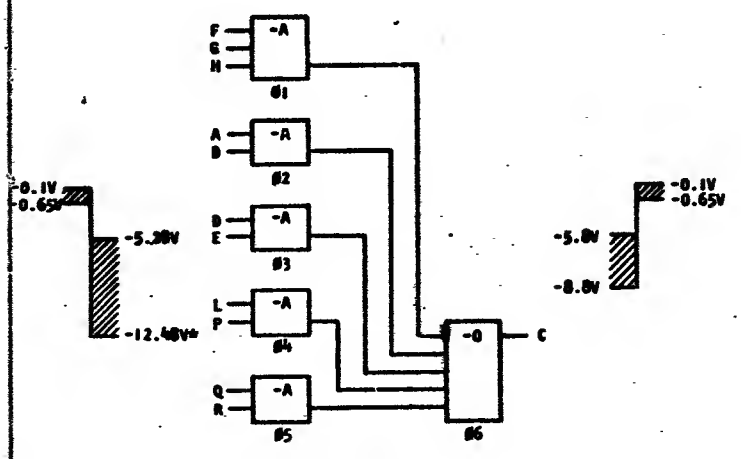
C

AXH-

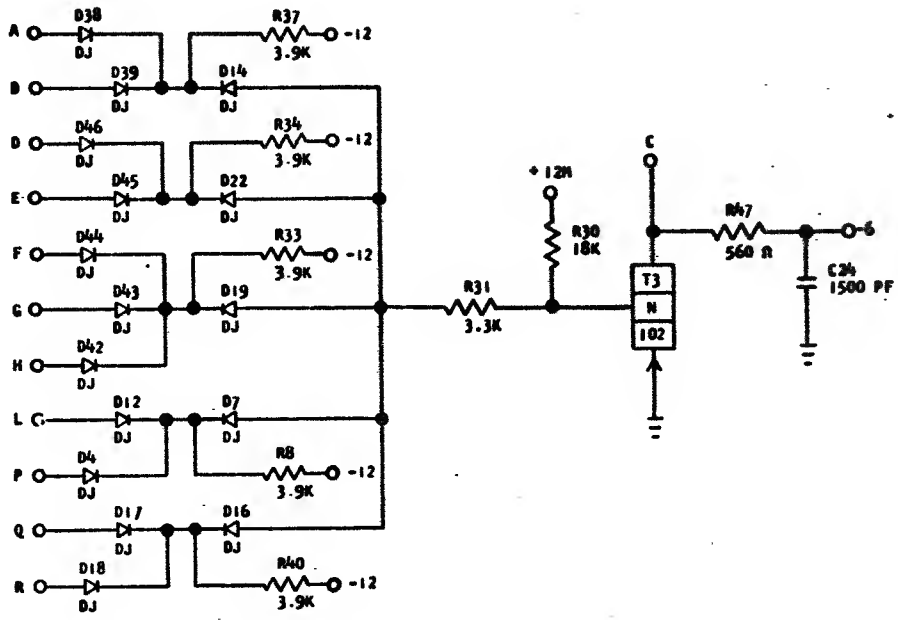
P/N: 372207 EC: 0114295

REFERENCE DRAWING
PRODUCTION DRAWING 372207

SDTDL LS FOUR 2-WAY, ONE 3-WAY NEGATIVE AND-NEGATIVE OR LOGIC BLOCKS WITH LOADS



*FUNCTION OF LOAD



OTHER DESIGNATIONS:

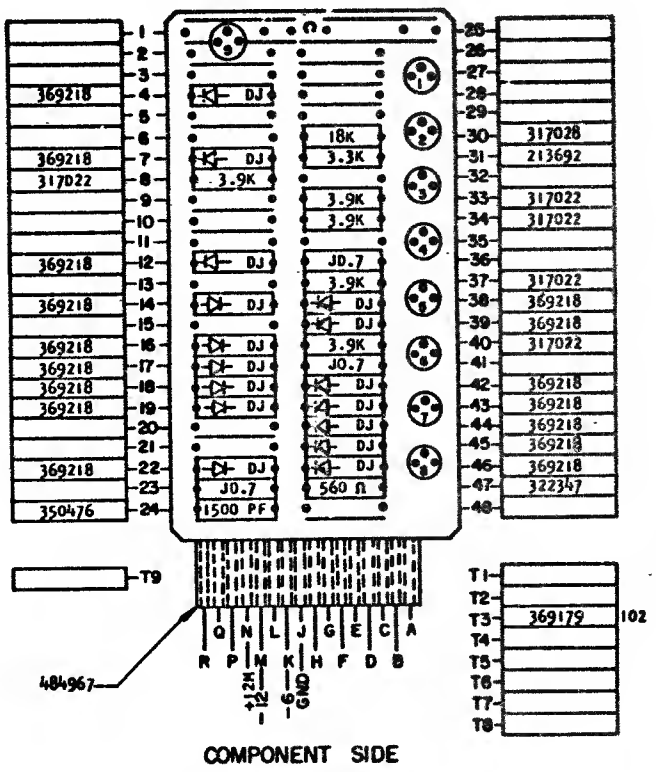
CONF. 1-5 +0
CONF. 6 +A,-00,+AA,-0A,+A0

SEQUENCE OF OPERATION

1. PINS A AND B MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
2. PINS F,G AND H MUST BE DOWN TO HAVE A DOWN LEVEL AT D19.
3. A DOWN LEVEL AT D7 OR D14 OR D16 OR D19 OR D22 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER A OR B UP WILL CAUSE AN UP LEVEL AT D14.
5. EITHER F OR G OR H UP WILL CAUSE AN UP LEVEL AT D19.
6. THE LEVELS AT D14,D22,D19,D7 AND D16 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734313
NAME SDTDL LS 4 2-WAY, 1 3-WAY NEG AND-NEG OR LOGIC BLOCKS WITH LOADS						3-25-63	116800						
DESIGN			MODEL	SMS 1440									
DETAIL			SCALE	NONE									
CHECK			DRAW	MDE	12-12-62								
APPRO		3-25-63	CHECK										

C

2-0

734374

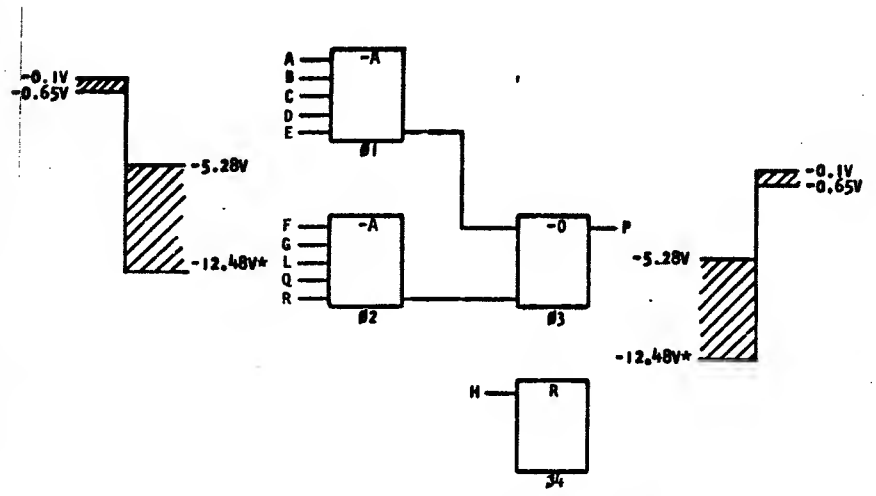
AXK—

P/N: 372209 EC: 0116177

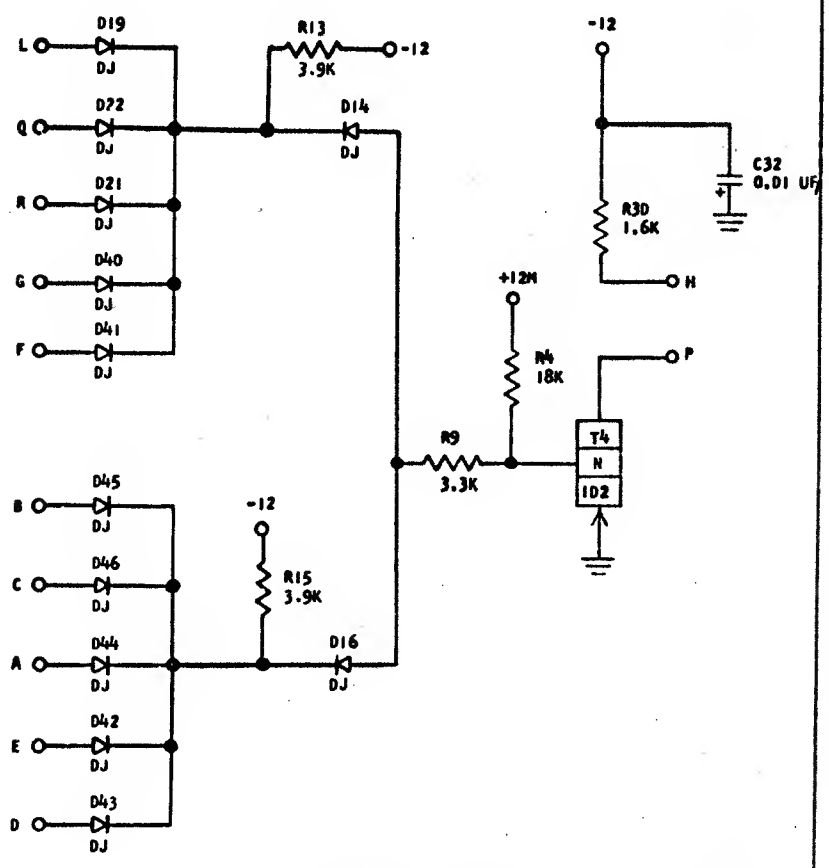
734374

REFERENCE DRAWING
PRODUCTION DRAWING 372209

SDTDL LS TWO 5-WAY NEGATIVE AND - NEGATIVE OR LOGIC BLOCKS WITH OR WITHOUT LOADS



* FUNCTION OF LOAD



OTHER DESIGNATIONS

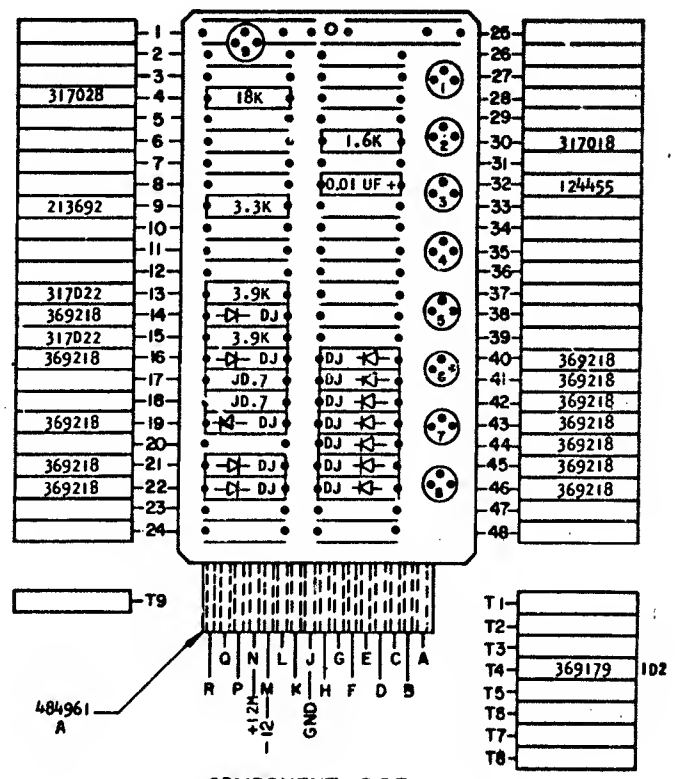
CONF. 1, 2 +0
CONF. 3 +A, -00, +AA, -0A, +A0

SEQUENCE OF OPERATION

1. PINS A, B, C, D AND E MUST BE DOWN TO HAVE A DOWN LEVEL AT D16.
2. PINS F, G, L, Q AND R MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
3. A DOWN LEVEL AT D14 OR D16 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER A, B, C, D OR E UP WILL CAUSE AN UP LEVEL AT D16.
5. EITHER F, G, L, Q OR R UP WILL CAUSE AN UP LEVEL AT D14.
6. THE LEVELS AT D14 AND D16 MUST BOTH BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734374
NAME	SDTDL LS TWO 5-WAY NEG AND-					3-25-63	116800						
	NEG OR LOGIC BLOCKS W OR W/O LOADS					4-10-63	116177	MDL					
DESIGN			MODEL	SMS 1440									
DETAIL			SCALE	NONE									
CHECK			DRAW	MDE	2-7-63								
APPRD	JCG	3-25-63	CHECK										

C

2-0

734318

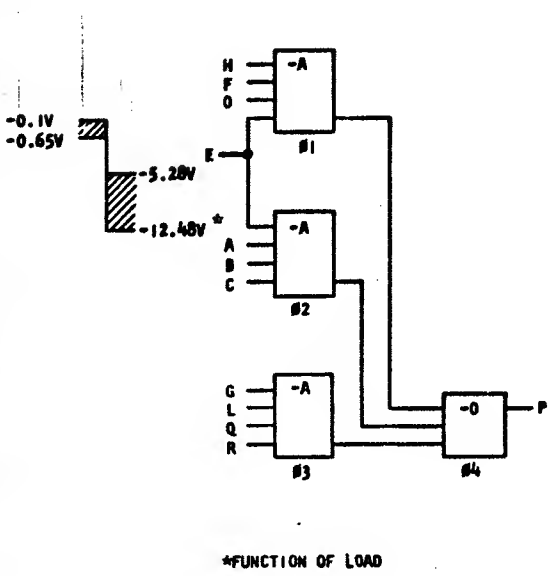
AXN-

P/N: 372212 EC: 0114296

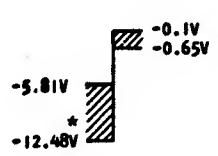
734318

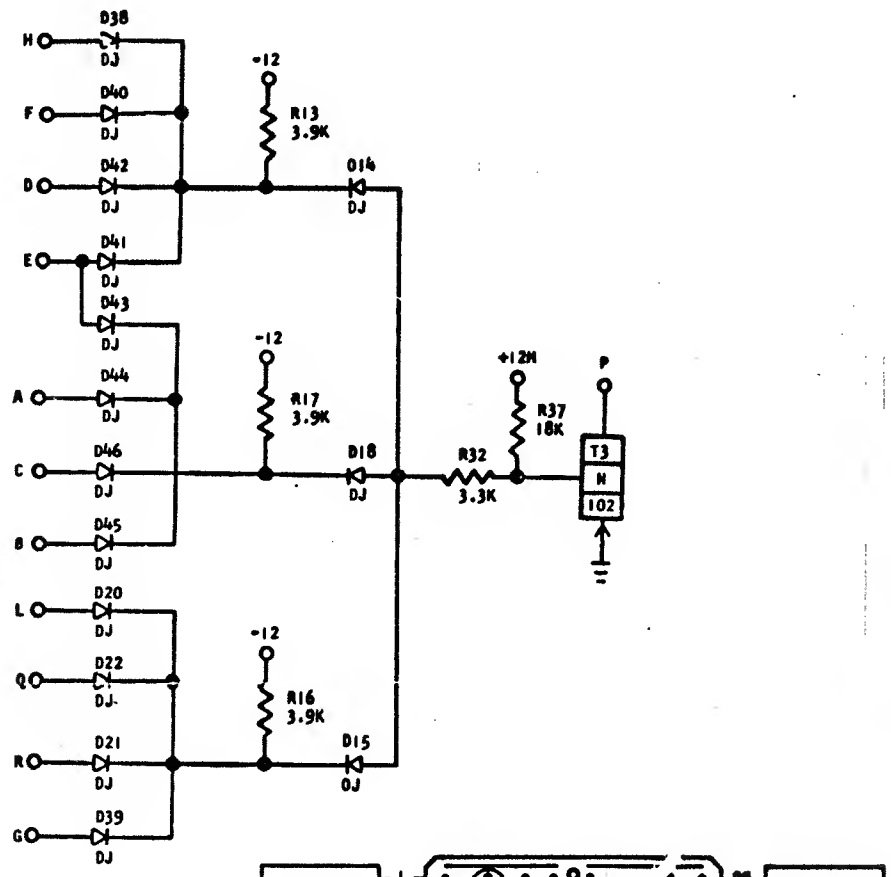
REFERENCE DRAWING
PRODUCTION DRAWING 372212

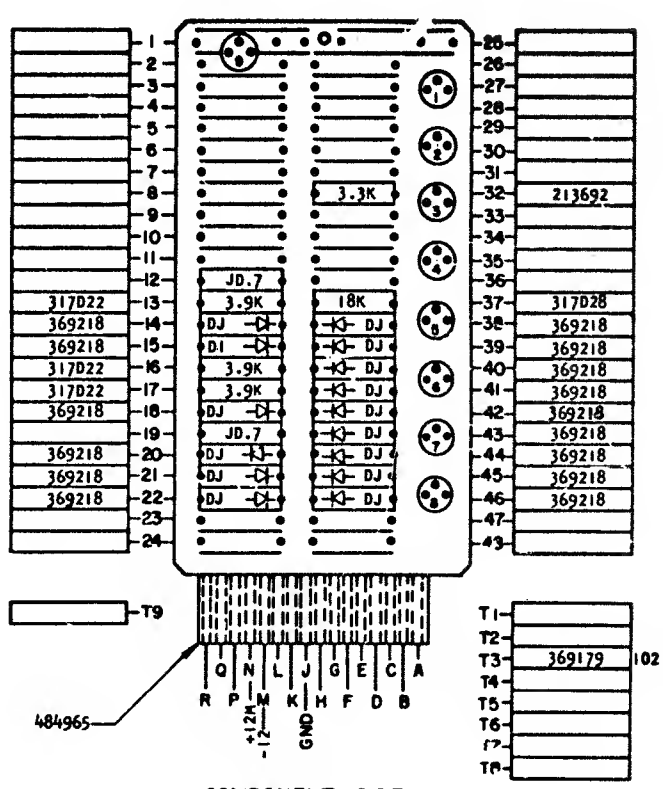
SDTDL LS THREE 4-WAY NEGATIVE AND-NEGATIVE OR LOGIC BLOCKS WITHOUT LOADS



*FUNCTION OF LOAD







OTHER DESIGNATIONS:

CONF. 1-3 +0
CONF. 4 +A,-00,+AA,-0A,+.0

SEQUENCE OF OPERATION

1. PINS A,B,C AND E MUST BE DOWN TO HAVE A DOWN LEVEL AT D18.
2. PINS G,L,Q AND R MUST BE DOWN TO HAVE A DOWN LEVEL AT D15.
3. A DOWN LEVEL AT D14, D15 OR D18 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER A,B,C OR E UP WILL CAUSE AN UP LEVEL AT D18.
5. EITHER G,L,Q OR R UP WILL CAUSE AN UP LEVEL AT D15.
6. THE LEVELS AT D18, D15 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	70	240*
TURN OFF (NSEC)	110	515**

*THIS DELAY CAN INCREASE TO 280 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 570 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734318
NAME	SDTDL LS 3 4-WAY NEG AND-NEG OR LOGIC BLOCKS WITHOUT LOADS					3-25-63	116800						
DESIGN			MODEL	SMS 1440									
DETAIL			SCALE	NONE									
CHECK			DRAW	MDE	12-19-62								
APPRO	KGJ	3-25-63	CHECK										

C

734319

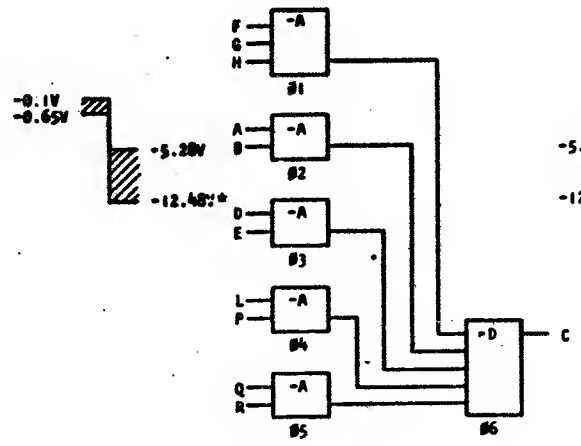
734319

AXP-

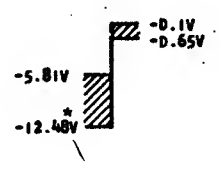
P/N: 372213 EC: 0114296

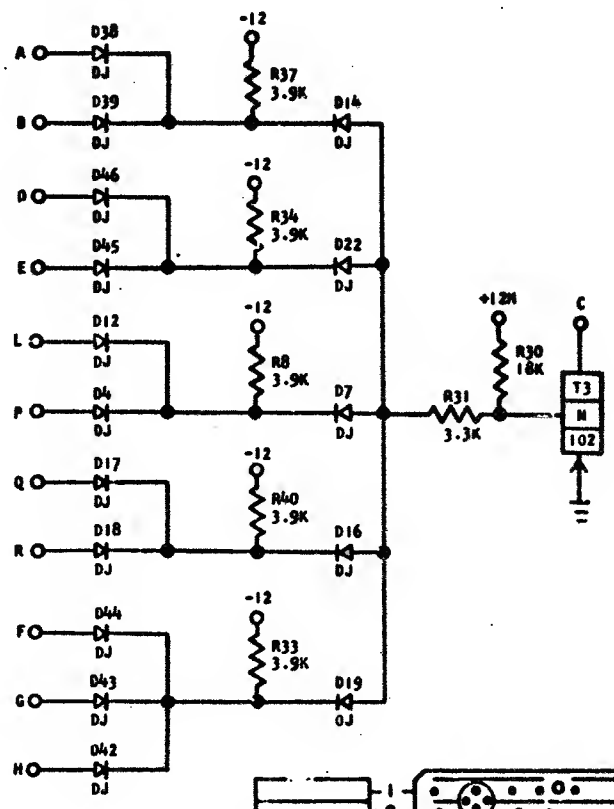
REFERENCE DRAWING
PRODUCTION DRAWING 372213

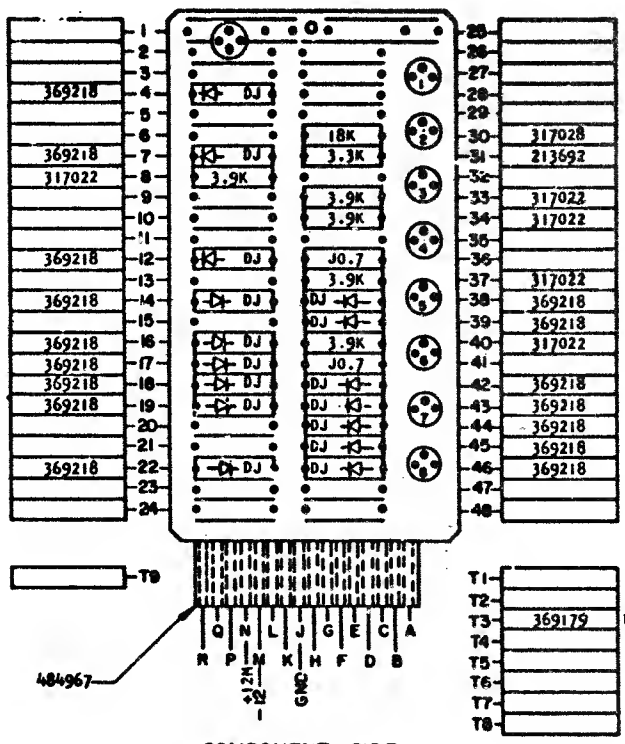
SDTDL LS FOUR 2-WAY, ONE 3-WAY NEGATIVE AND-NEGATIVE OR LOGIC BLOCKS WITHOUT LOADS



*FUNCTION OF LOAD







COMPONENT SIDE

OTHER DESIGNATIONS:

CONF. 1-5 +0
CONF. 6 +A, -00, +AA, -0A, +A0

SEQUENCE OF OPERATION

1. PINS A AND B MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
2. PINS F,G AND H MUST BE DOWN TO HAVE A DOWN LEVEL AT D19.
3. A DOWN LEVEL AT D7, D14, D16, D19 OR D22 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER A OR B UP WILL CAUSE AN UP LEVEL AT D14.
5. EITHER F,G OR H UP WILL CAUSE AN UP LEVEL AT D19.
6. THE LEVELS AT D7, D14, D16, D19 AND D22 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	7D	240*
TURN OFF (NSEC)	11D	515**

*THIS DELAY CAN INCREASE TO 280 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 570 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	SDTDL LS 4 2-WAY, 1 3-WAY NEG AND-NEG OR LOGIC BLOCKS W/O LOADS				3-25-63	116800						734319
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE 12-19-62								
APPRD	RC-3	3-25-63	CHECK									

C

734320

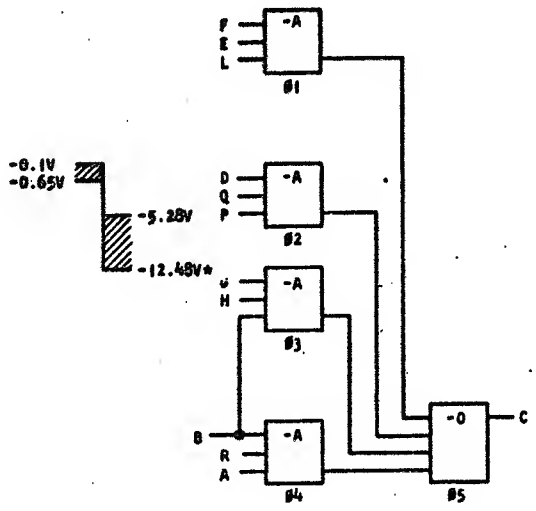
734320

AXQ-

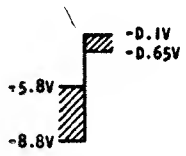
P/N: 372214 EC: 0114296

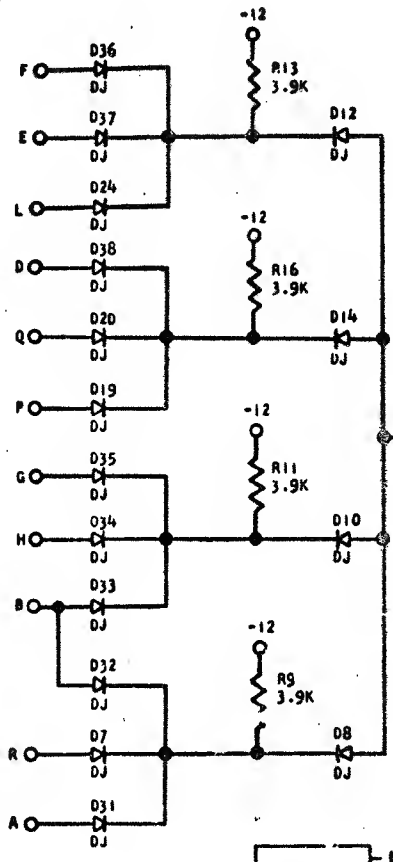
REFERENCE DRAWING
PRODUCTION DRAWING 372214

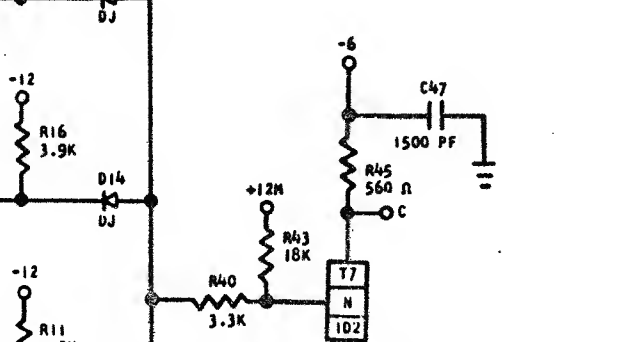
SDTDL LS FOUR 3-WAY NEGATIVE AND-NEGATIVE OR LOGIC BLOCKS WITH LOADS

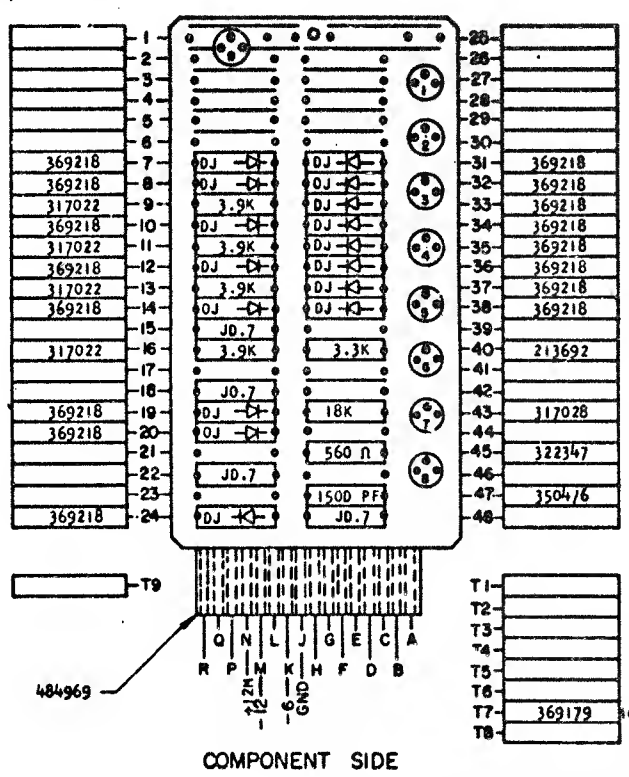


*FUNCTION OF LOAD









COMPONENT SIDE

OTHER DESIGNATIONS:

CONF. 1-4 +0
CONF. 5 +A,-00,+AA,-0A,+A0

SEQUENCE OF OPERATION

1. PINS F, E AND L MUST BE DOWN TO HAVE A DOWN LEVEL AT D12.
2. PINS D, Q AND P MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
3. A DOWN LEVEL AT D8, D10, D12 OR D14 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER F, E OR L UP WILL CAUSE AN UP LEVEL AT D12.
5. EITHER D, Q OR P UP WILL CAUSE AN UP LEVEL AT D14.
6. THE LEVELS AT D8, D10, D12 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME SDTDL LS 4 3-WAY NEG AND-NEG OR LOGIC BLOCKS WITH LOADS					3-25-63	116800						734320
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			DRAW	HDE 12-19-62								
APPRO		3-25-63	CHECK									

C

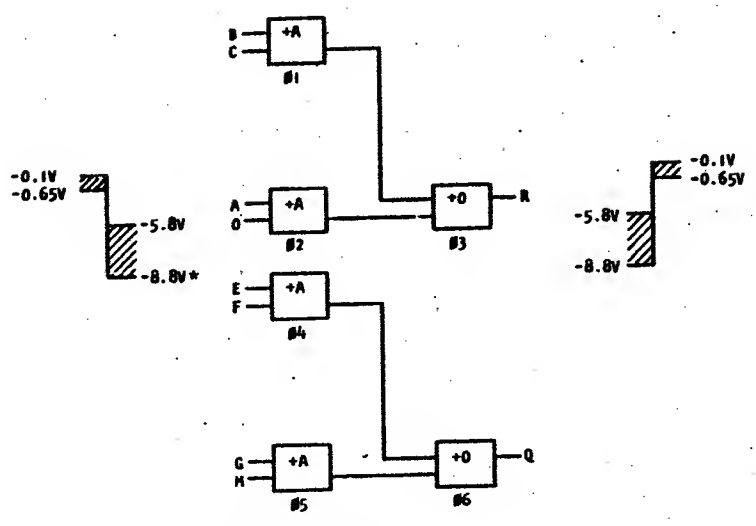
734322

AXR-

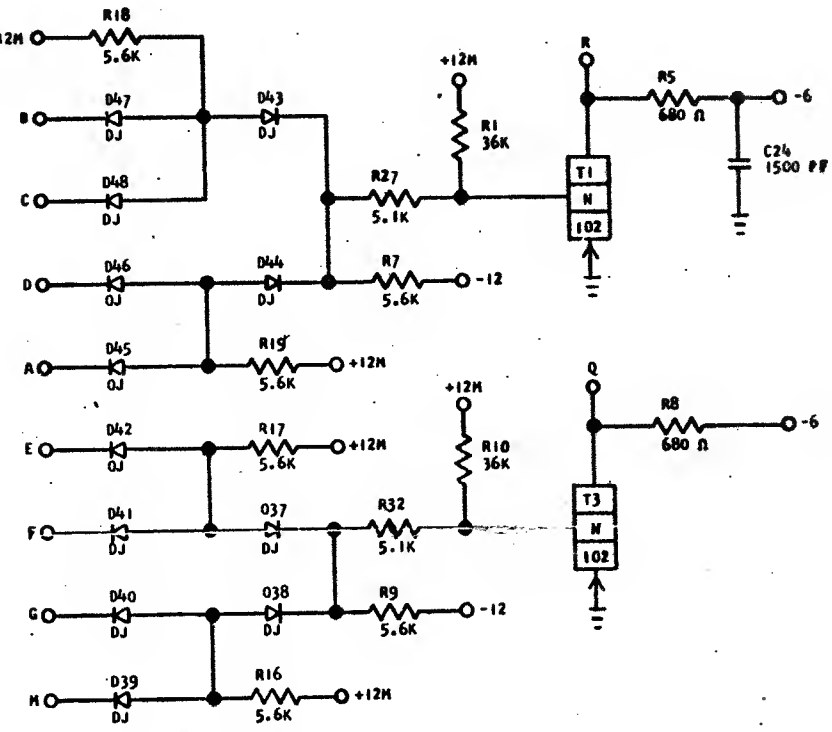
P/N: 372240 EC: 0114320

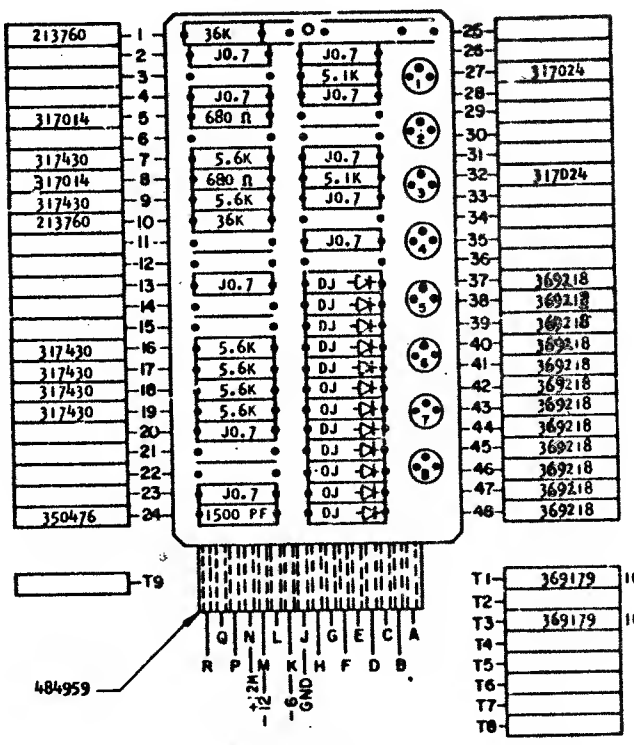
REFERENCE DRAWING
PRODUCTION DRAWING 372240

SDTDL LS TWO 2-WAY POSITIVE AND-POSITIVE OR LOGIC BLOCKS WITH LOADS



* FUNCTION OF LOAD





COMPONENT SIDE

OTHER DESIGNATIONS.

CONF. 1,2,4,5 -O
CONF. 3,6 -A, +OA, -AO, +OO, -AA

SEQUENCE OF OPERATION

1. PINS B AND C MUST BE UP TO HAVE AN UP LEVEL AT D43.
2. PINS D AND A MUST BE UP TO HAVE AN UP LEVEL AT D44.
3. EITHER LEVEL UP AT D43 OR D44 WILL CAUSE THE TRANSISTOR TO TURN OFF, THE OUTPUT WILL BE DOWN.
4. EITHER B OR C DOWN WILL CAUSE A DOWN LEVEL AT D43.
5. EITHER D OR A DOWN WILL CAUSE A DOWN LEVEL AT D44.
6. BOTH LEVELS AT D43 AND D44 MUST BE DOWN TO TURN THE TRANSISTOR ON, THE OUTPUT WILL BE UP.

DELAY

	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734322
NAME	SDTOL LS 2 2-WAY POS AND-POS OR LOGIC BLOCKS WITH LOADS				3-25-63	116800						
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE 12-19-62								
APPRO		3-25-63	CHECK									

C

22

734323

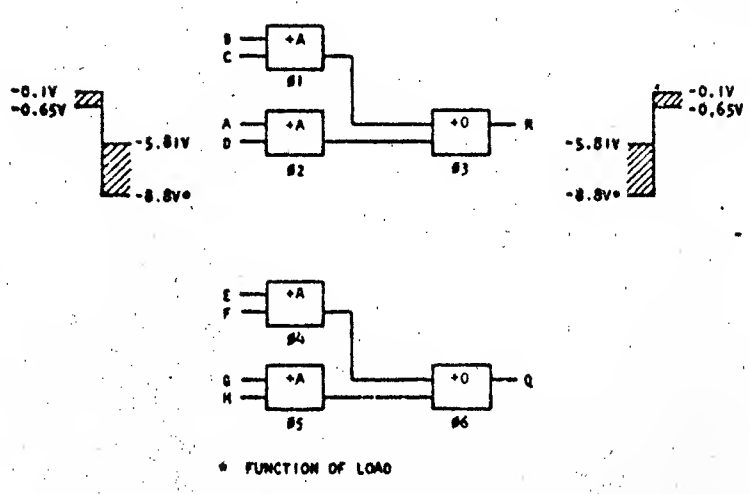
734323

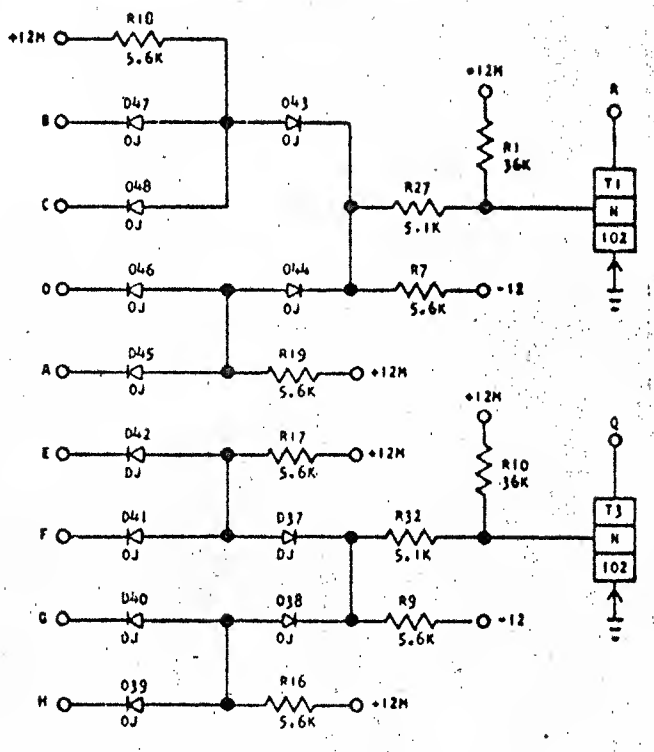
AXS-

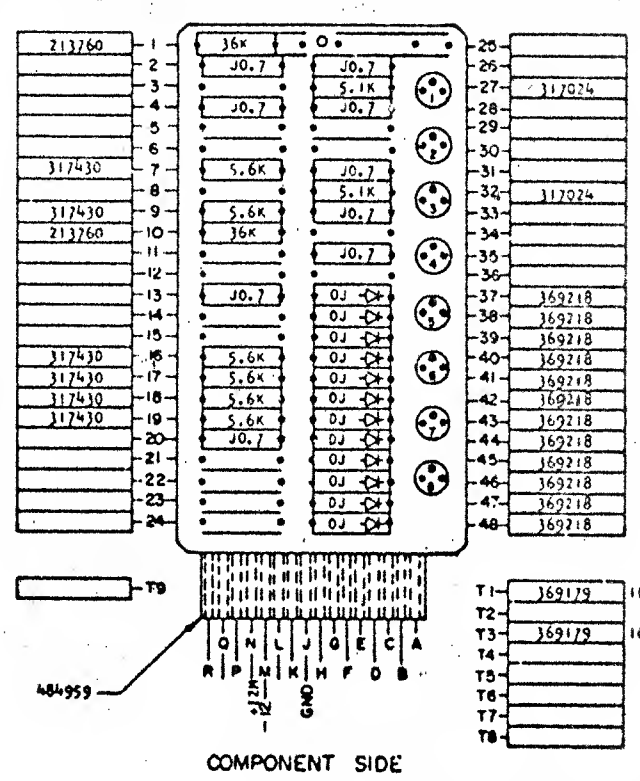
P/N: 372241 EC: 0114320

REFERENCE DRAWING
PRODUCTION DRAWING 372241

SDTDL LS TWO 2-WAY POSITIVE AND-POSITIVE OR LOGIC BLOCKS WITHOUT LOADS







OTHER DESIGNATIONS:

CONF. 1,2,4,5 -0
CONF. 3,6 -A,+0A,-A0,+00,-AA

SEQUENCE OF OPERATION

1. PINS B AND C MUST BE UP TO HAVE AN UP LEVEL AT 043.
2. PINS D AND A MUST BE UP TO HAVE AN UP LEVEL AT 044.
3. EITHER LEVEL UP AT 043 OR 044 WILL CAUSE THE TRANSISTOR TO TURN OFF, THE OUTPUT WILL BE DOWN.
4. EITHER B OR C DOWN WILL CAUSE A DOWN LEVEL AT 043.
5. EITHER D OR A DOWN WILL CAUSE A DOWN LEVEL AT 044.
6. BOTH LEVELS AT 043 AND 044 MUST BE DOWN TO TURN THE TRANSISTOR ON, THE OUTPUT WILL BE UP.

DELAY

WITH 680 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	70	240*
TURN OFF (NSEC)	110	515**

*THIS DELAY CAN INCREASE TO 280 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 570 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME SDTDL LS 2 2-WAY POS AND-POS OR LOGIC BLOCKS WITHOUT LOADS					3-25-63	116800					
DESIGN			MODEL	SMS 1440							
DETAIL			SCALE	NONE							
CHECK			DRAW	MOE 12-19-62							
APPRO		3-25-63	CHECK								

734323

C

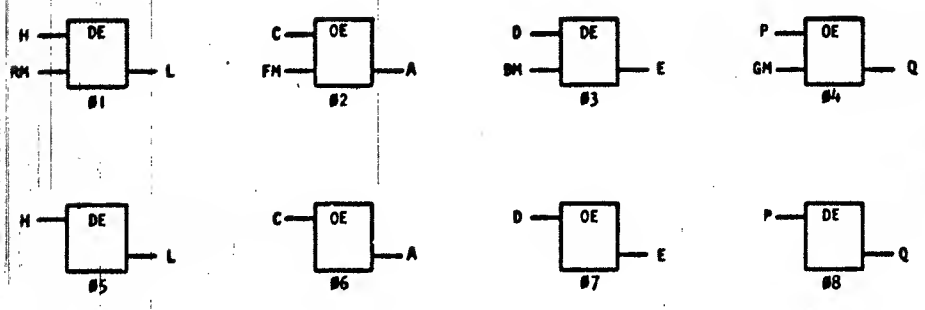
734338

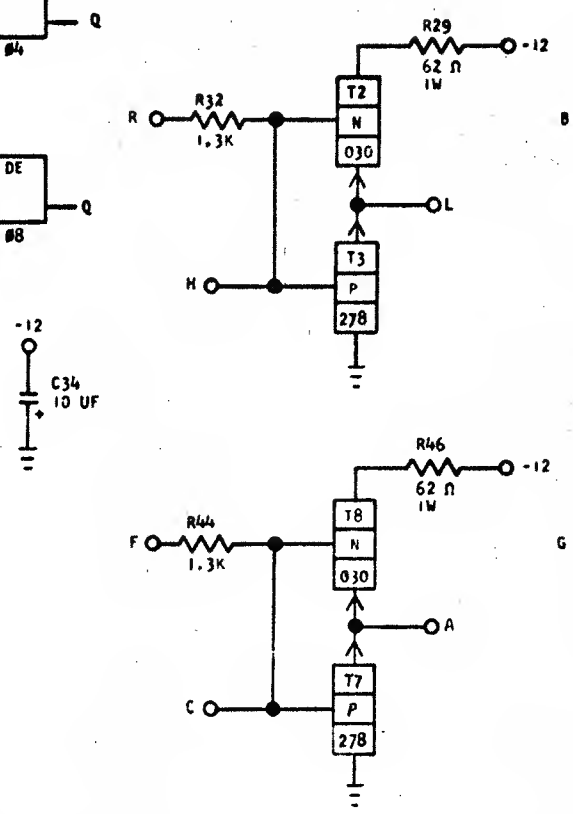
AXV—

P/N: 372244

REFERENCE DRAWING
PRODUCTION DRAWING 372244

COMPLEMENTARY EMITTER FOLLOWER





SEQUENCE OF OPERATION

1. INPUT UP: TRANSISTOR (T3) ON, OUTPUT UP.
2. INPUT OOWN: TRANSISTOR (T2) ON, OUTPUT DOWN.

NOTES: 1. CONF. #1-#4 MAY ONLY BE ORIVEN BY UNLOAOEO BLOCKS DUE TO THE 1.3K RESISTOR TIEO TO -12V.

2. CONF. #5-#8 ARE USEO WHEN DRIVEN BY A CLAMPEO LOGIC BLOCK, IP, OR TRIGGER.

PINS	SIGNAL NAME		WAVESHAPE	LEVELS	MIN	MAX
H	Y	INPUT		UP	-.65V	-.05V
				DOWN	-6V	*
L	Y	OUTPUT		UP	-1.25V	-.05V
				DOWN	-6.71V[1]	-6.71V[1]
H	Y	INPUT		UP	-.65V	-.05V
				DOWN	-6V	*
L	Y	OUTPUT		UP	-1.25V	-.05V
				DOWN	-5.51V	-6.69V[2]

* FUNCTION OF CURRENT SWITCHED.

1. ORIVEN BY LOGIC BLOCK.
2. DRIVEN BY IP, TRIGGER OR CLAMPED LOGIC BLOCK.

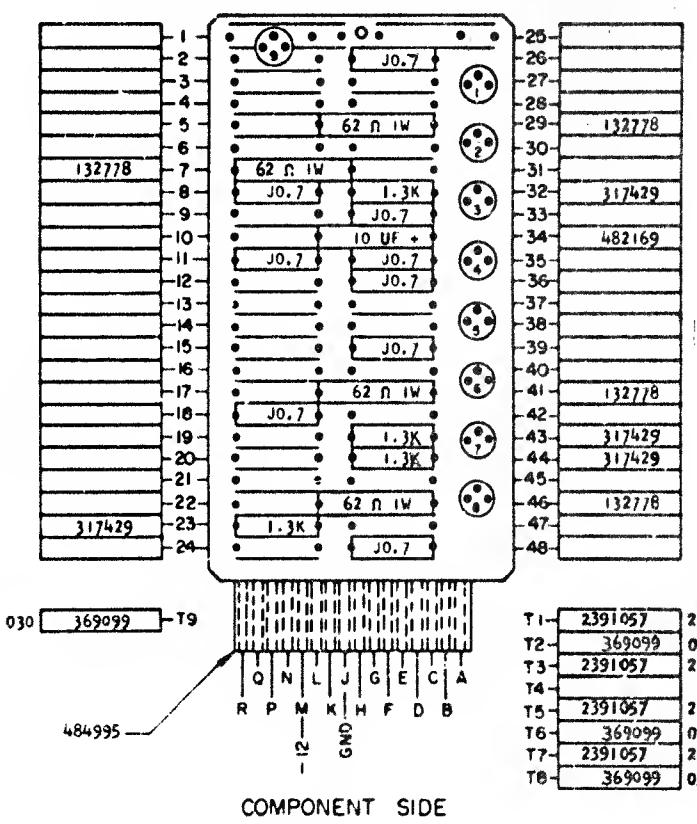
DELAY-MAXIMUM

LOW SPEED DRIVERS:

	TURN ON (NSEC)	TURN OFF (NSEC)
LOGIC BLOCK	70	50
CLAMPED LOGIC BLOCK	24	28.
I.P.	36	20

HIGH SPEED DRIVERS:

	TURN ON (NSEC)	TURN OFF (NSEC)
LOGIC BLOCK	46	52
CLAMPED LOGIC BLOCK	39	32
I.P.	56	21



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734338
NAME	COMPLEMENTARY EMITTER FOLLOWER				3-25-63	116800						
					11-21-64	122721	GLK					
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE 1-3-63								
APPRO	[illegible] 3-25-63		CHECK									

C

734321

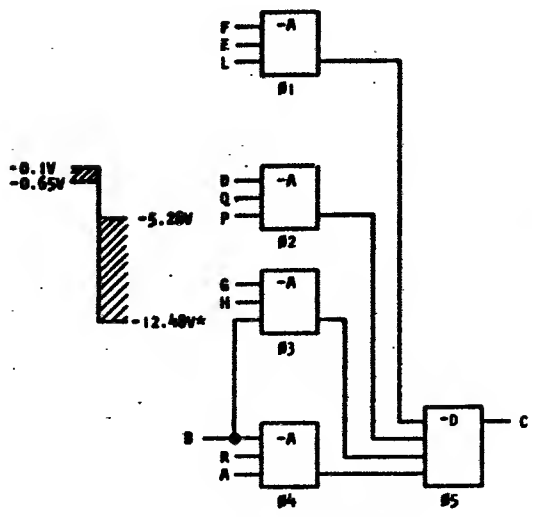
734321

AXW-

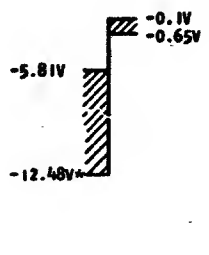
P/N: 372236 EC: 0114319

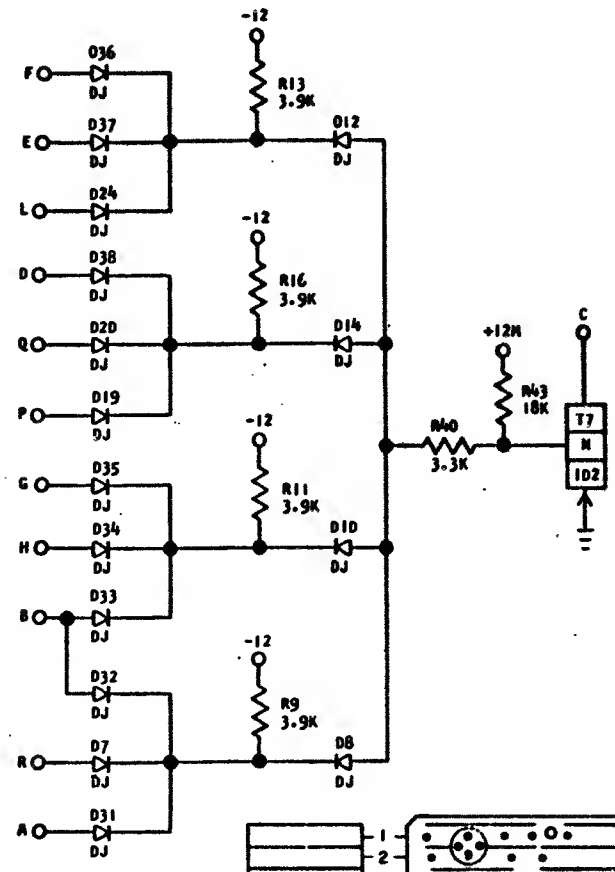
REFERENCE DRAWING
PRODUCTION DRAWING 372236

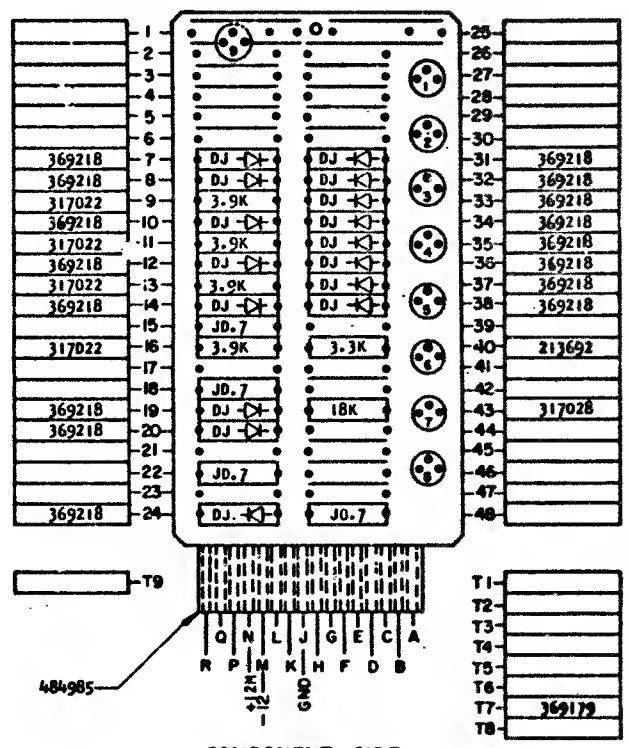
SDTDL LS FOUR 3-WAY NEGATIVE AND-NEGATIVE OR LOGIC BLOCKS WITHOUT LOADS



* FUNCTION OF LOAD







COMPONENT SIDE

OTHER DESIGNATIONS:

CONF. 1-4 +0
CONF. 5 +A,-BD,+AA,-DA,+AD

SEQUENCE OF OPERATION

1. PINS F,E AND L MUST BE DOWN TO HAVE A DOWN LEVEL AT D12.
2. PINS O,Q AND P MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
3. A DOWN LEVEL AT D8, D10, D12 OR D14 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER F,E OR L UP WILL CAUSE AN UP LEVEL AT D12.
5. EITHER O,Q OR P UP WILL CAUSE AN UP LEVEL AT D14.
6. THE LEVELS AT D8, D10, D12 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	70	240*
TURN OFF (NSEC)	110	515**

*THIS DELAY CAN INCREASE TO 280 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 570 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL LS 4 3-WAY NEG AND-NEG OR LOGIC BLOCKS WITHOUT LOADS				3-25-63	116800					
DESIGN			MODEL	SMS 1440							
DETAIL			SCALE	NONE							
CHECK			DRAW	MDE 12-19-62							
APPRD	RCA	3-25-63	CHECK								

734321

C

734347

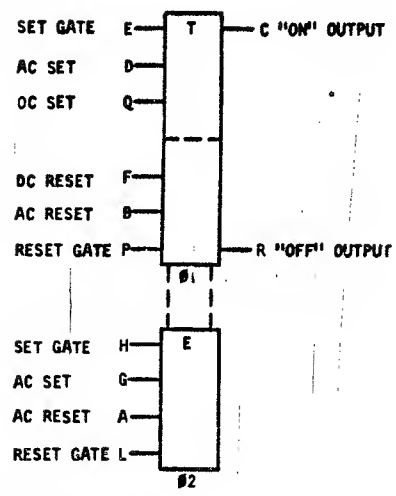
734347

AXZ-

P/N: 372239

REFERENCE DRAWING
PRODUCTION DRAWING 372239

SDTDL LOW SPEED TRIGGER



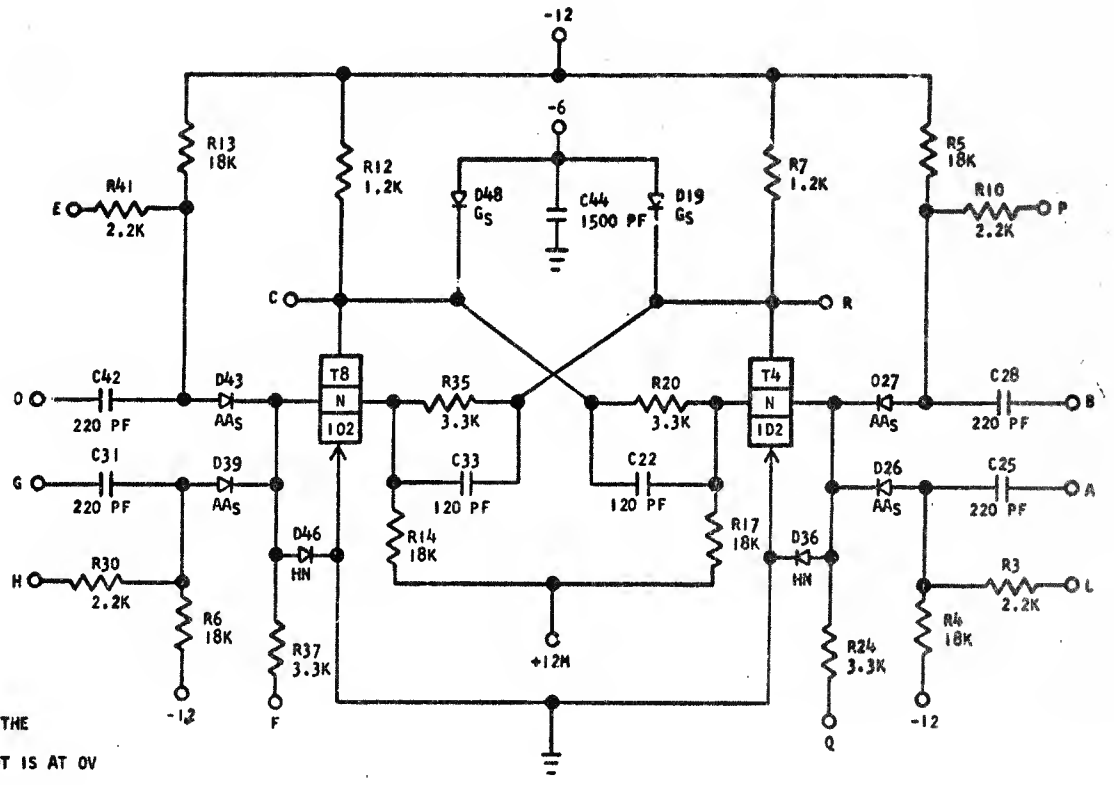
OTHER DESIGNATIONS
TB

SEQUENCE OF OPERATION

1. WHEN THE TRIGGER IS SET, THE "ON" OUTPUT IS AT -6V AND THE "OFF" OUTPUT IS OV.
2. WHEN THE TRIGGER IS IN A RESET CONDITION THE "ON" OUTPUT IS AT OV AND THE "DFF" OUTPUT IS AT -6V.
3. TRIGGER IS SET BY
   A) A NEGATIVE VOLTAGE LEVEL APPLIED TO THE DC SET INPUT OR
   B) AN UP LEVEL AT THE SET GATE INPUT IN CONJUNCTION WITH A POSITIVE SHIFT AT THE AC SET INPUT.
4. TRIGGER IS RESET BY
   A) A NEGATIVE VOLTAGE LEVEL AT THE DC RESET INPUT DR
   B) AN UP LEVEL AT THE RESET GATE INPUT IN CONJUNCTION WITH A POSITIVE SHIFT AT THE AC RESET INPUT.

NOTES:

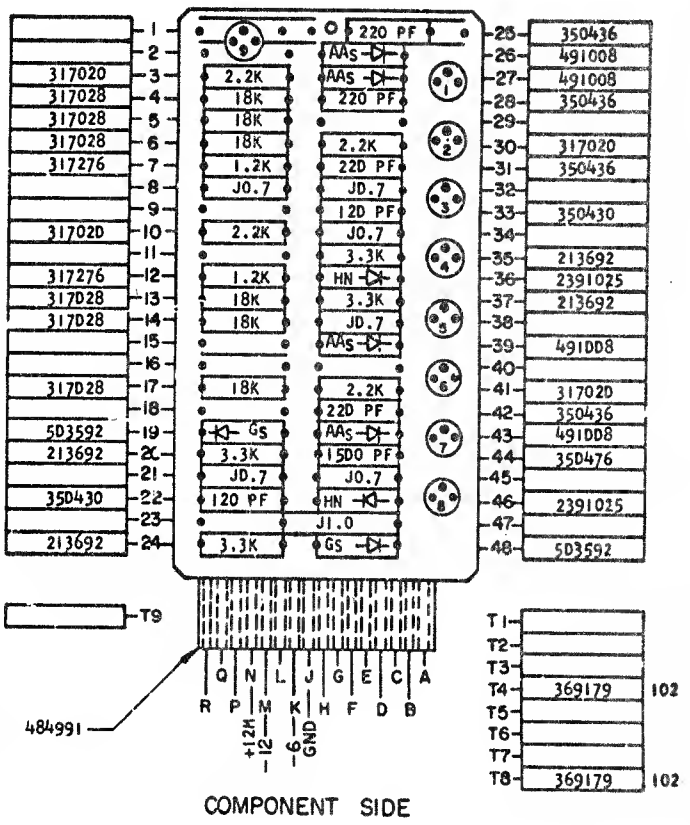
1. THE GATES MUST BE AT THE UP LEVEL 150 NS BEFORE THE AC SET ARRIVES.
2. THE AC SET SHDULD BE AT LEAST 70 NS WIDE AND ITS RISE TIME 70 NS OR LESS.



PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
E H	Y	SET GATE		UP	-.65V	-.05V
				DOWN	-5.81V	-7.64V
D G	Y	AC SET		UP	-.65V	-.05V
				DDWN	-5.81V	-7.64V
B A	Y	AC RESET		UP	-.65V	-.05V
				DOWN	-5.81V	-7.64V
P L	Y	RESET GATE		UP	-.65V	-.05V
				DOWN	-5.81V	-7.64V
Q	Y	OC SET		UP	-.65V	-.05V
				DOWN	-6.26V	-7.64V
F	Y	DC RESET		UP	-.65V	-.05V
				DOWN	-6.26V	-7.64V
C	Y	"ON" OUTPUT		UP	-.65V	-.05V
				DOWN	-6.26V	-7.64V
R	Y	"OFF" OUTPUT		UP	-.65V	-.05V
				DDWN	-6.26V	-7.64V

DELAY - NSEC

	TON MAX	TON MIN	TRISE MAX	TRISE MIN	TOFF MAX	TOFF MIN	TFALL MAX	TFALL MIN
BINARY OPERATION:	340	40	50	25	825	175	635	155
GATED:	350	35	50	20	685	125	475	110



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.													
NAME	SDTDL LOW SPEED TRIGGER												
DESIGN			MODEL	SMS 1440									
DETAIL			SCALE	NONE									
CHECK			DRAW	MDE	1-9-63								
APPRO		3-25-63	CHECK										

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
3-25-63	116800					
CAUG66	127574	GLK				

734347

C

2-0

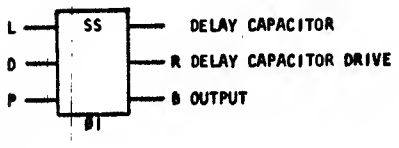
734405

AZK-

P/N: 372275

REFERENCE DRAWING
PRODUCTION DRAWING 372275

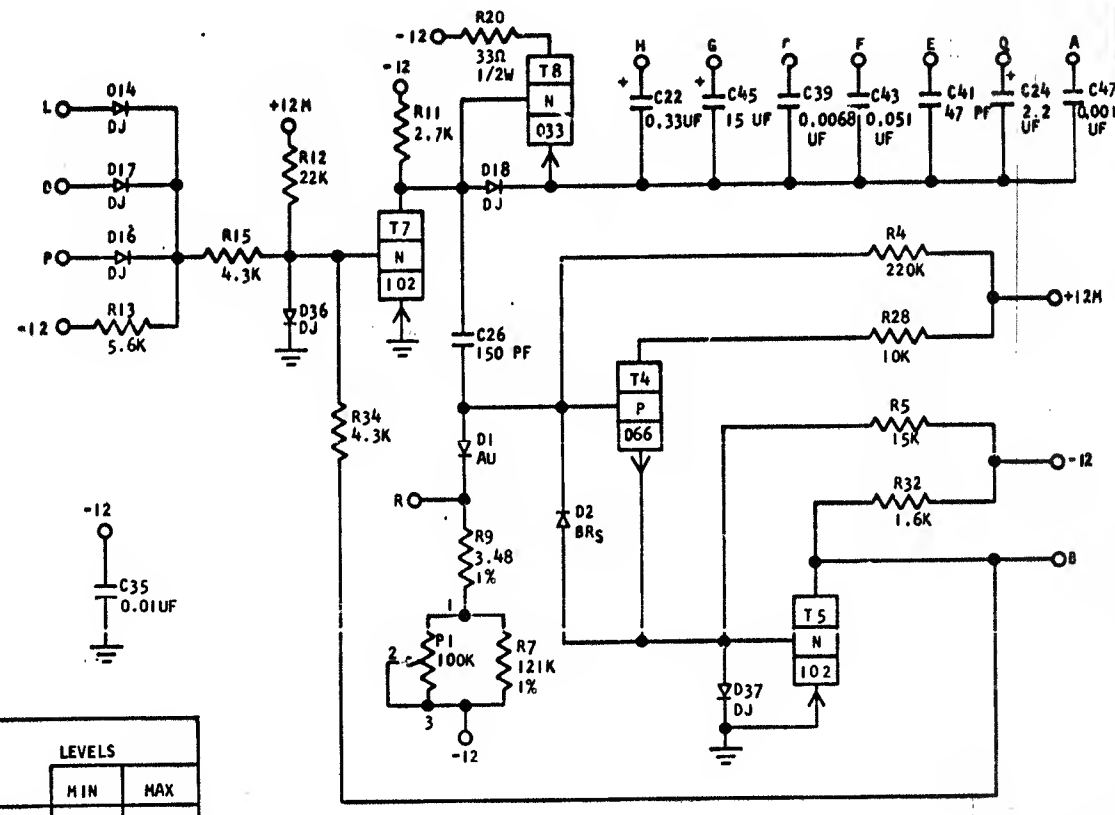
SDTDL SINGLE SHOT



SEQUENCE OF OPERATION

1. OPERATION IS INITIATED BY COINCIDENCE OF DOWN LEVELS ON PINS L, D, AND P. T7 TURNS ON AND ITS OUTPUT IS COUPLED THROUGH C26 TO TURN ON T4. T5 TURNS OFF AND THE OUTPUT IS DOWN FOR THE DURATION OF THE DELAY TIME.

2. RESET TO THE OFF CONDITION IS AUTOMATIC AT THE END OF THE DELAY TIME.

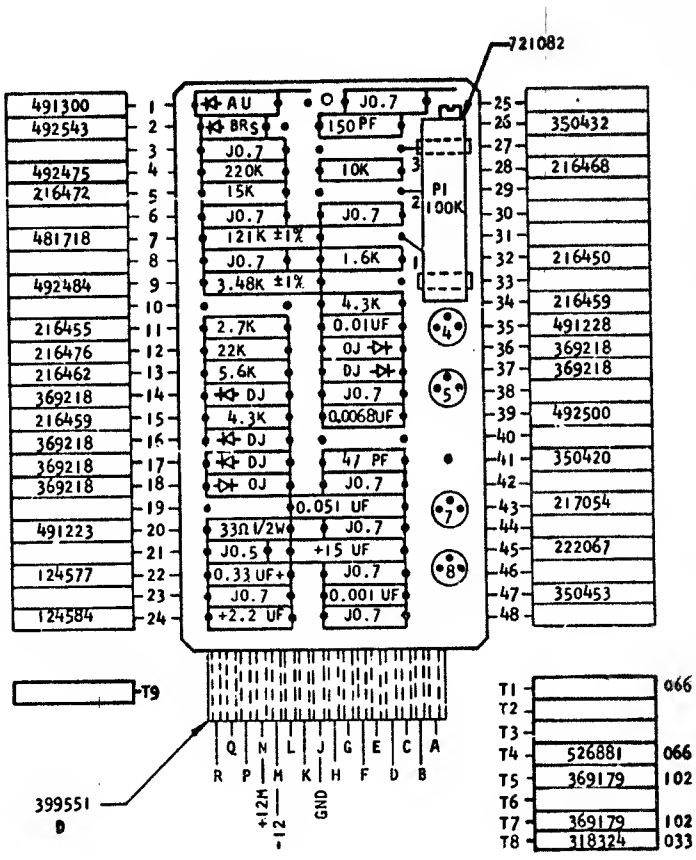


PINS	SIGNAL NAME		WAVESHAPE		LEVELS MIN	LEVELS MAX
L	Y	INPUT		UP	-.65V	+.24V
				DOWN	-5.81V	-12.48V
D	Y	INPUT		UP	-.65V	+.24V
				DOWN	-5.81V	-12.48V
P	Y	INPUT		UP	-.65V	+.24V
				DOWN	-5.81V	-12.48V
B	Y	INPUT	*DELAY TIME	UP	-.65V	-.05V
				DOWN	-5.81V	-9.51V

* THE DELAY TIME IS DETERMINED BY THE CAPACITOR WIRED TO PIN R AND THE SETTING OF THE DELAY POTENTIOMETER.

DELAY	MIN	MAX
T_{ON} (NSEC)	30	380
T_{OFF} (NSEC)	390	340

WIRE PIN R TO	FOR PULSE WIDTHS FROM	TO
E	.39 US	3.0 US
A	2.9 US	21 US
AC	21 US	167 US
F	143 US	1.1 MS
ACH	.94 MS	7.29 MS
HQ	7.4 MS	63 MS
GQ	51 MS	340 MS



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	SDTDL SINGLE SHOT					3-25-63	116800						734405
						12-11-63	119236						
DESIGN			MODEL	SMS 1440		8-31-64	121295						
DETAIL			SCALE	NONE		20JUL65	124792						
CHECK			DRAW	MOE	3-13-63	7JUN66	126392						
APPKD	KED	3-25-63	CHECK										

C

2-0

734380

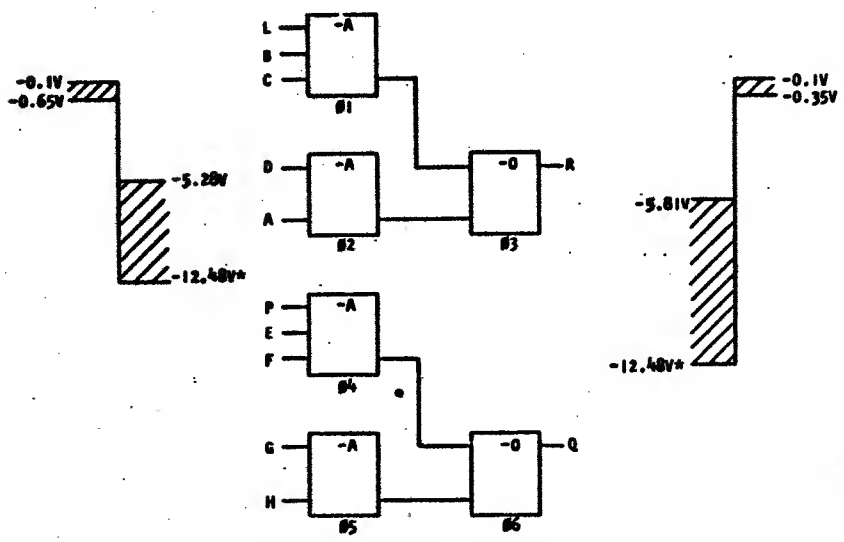
734380

CEX-

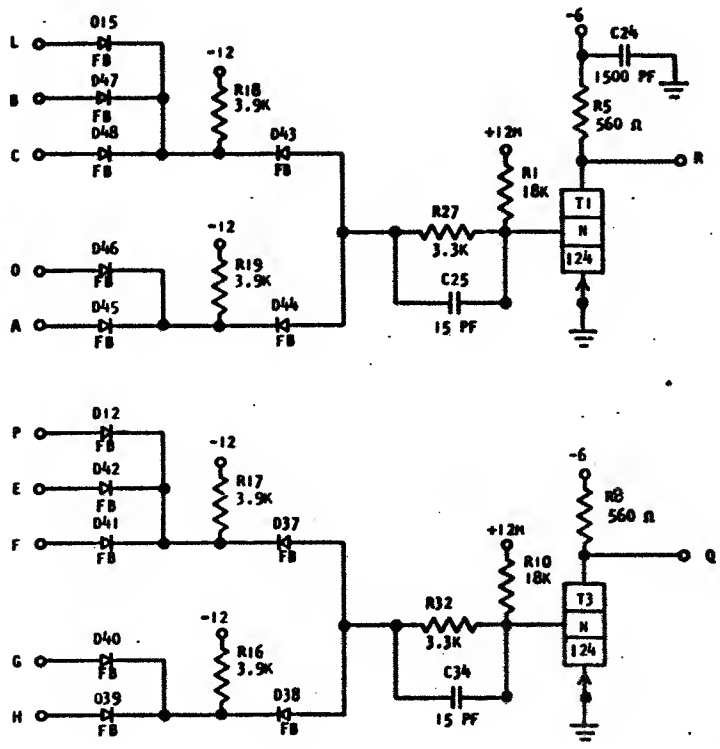
P/N: 372530 EC: 0116156

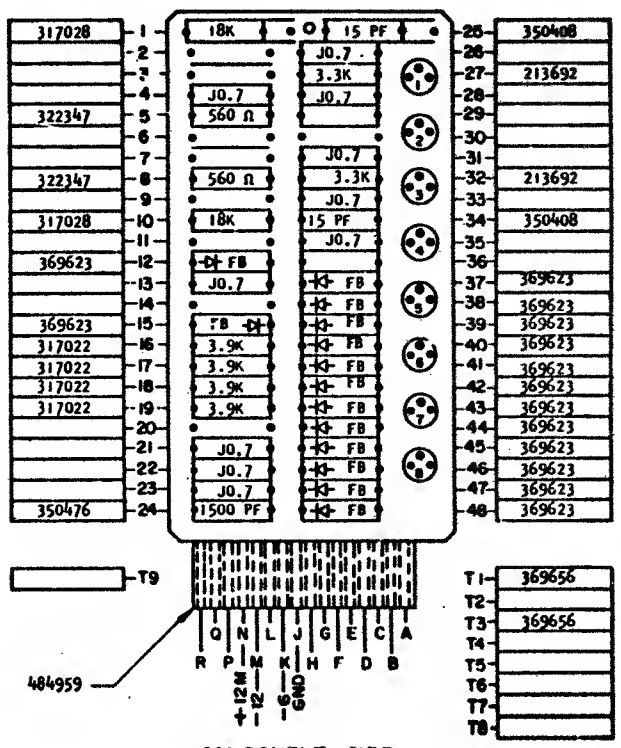
REFERENCE DRAWING
PRODUCTION DRAWING 372530

SDTDL HS ONE 2-WAY, ONE 3-WAY NEGATIVE AND - NEGATIVE OR LOGIC BLOCKS WITH LOADS



* FUNCTION OF LOAD





OTHER DESIGNATIONS

CONF. 1, 2, 4, 5	+0
CONF. 3, 6	+A, -00, +AA, -0A, +A0

SEQUENCE OF OPERATION

1. PINS L, B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D43.
2. PINS A AND D MUST BE DOWN TO HAVE A DOWN LEVEL AT D44.
3. EITHER DOWN LEVEL AT D43 OR D44 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER L, B OR C UP WILL CAUSE AN UP LEVEL AT D43.
5. EITHER D OR A UP WILL CAUSE AN UP LEVEL AT D44.
6. BOTH LEVELS AT D43 AND D44 MUST BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	15	280
TURN OFF (NSEC)	24	300

C

INTERNATIONAL BUSINESS MACHINES CORP.					DATE.	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734380
NAME	SDTOL HS 1 2-WAY, 1 3-WAY NEG AND-NEG OR LOGIC BLOCKS WITH LOADS				4-24-63	116800						
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			DRAW	HDE 2-8-63								
APPRO	[illegible]	4-24-63	CHECK									

2-0

734381

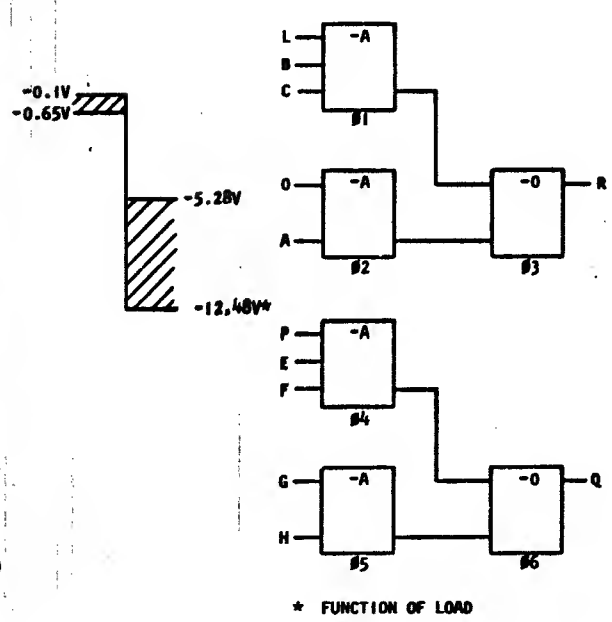
734381

CEY-

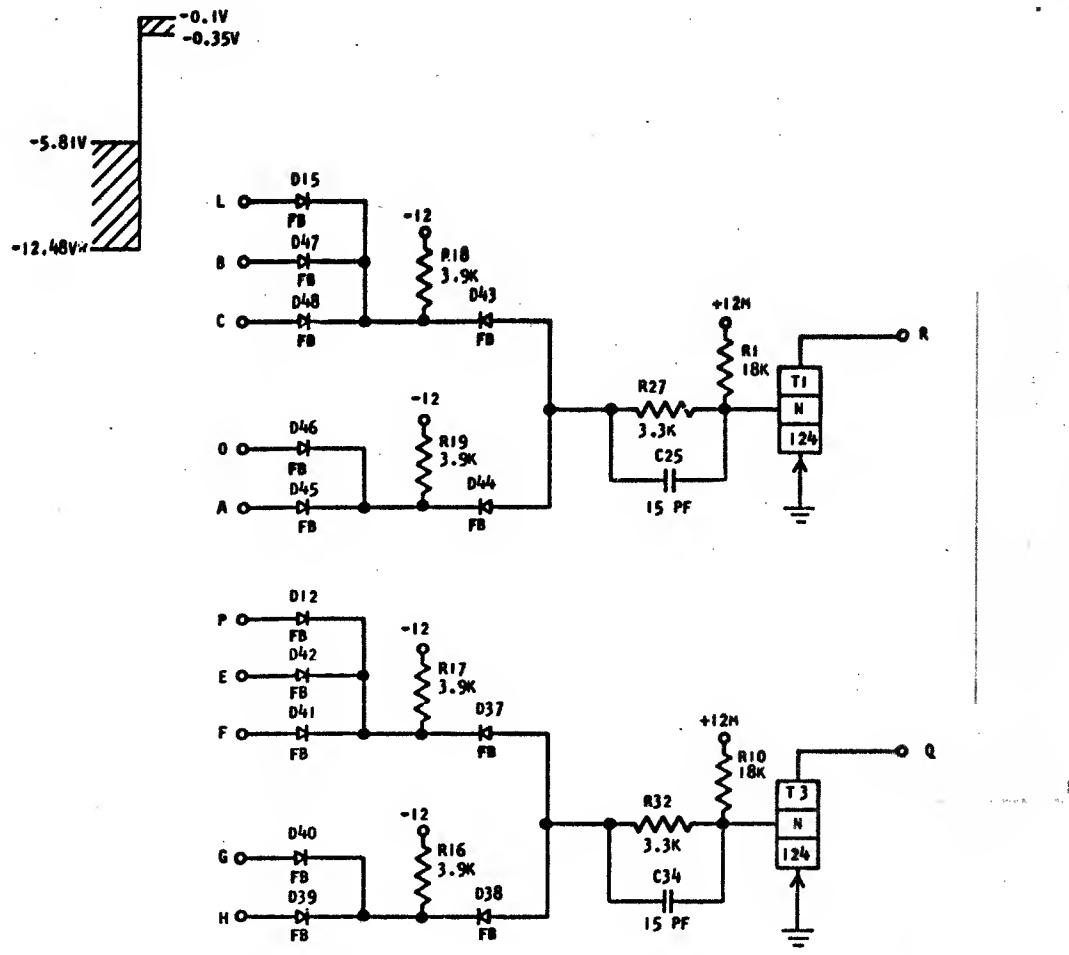
P/N: 372531 EC: 0116156

REFERENCE DRAWING
PRODUCTION DRAWING 372531

SDTDL HS ONE 2-WAY, ONE 3-WAY NEGATIVE AND - NEGATIVE OR LOGIC BLOCKS WITHOUT LOADS



* FUNCTION OF LOAD



OTHER DESIGNATIONS

CONF. 1, 2, 4, 5	+0
CONF. 3, 6	+A, -00, +AA, -0A, +A0

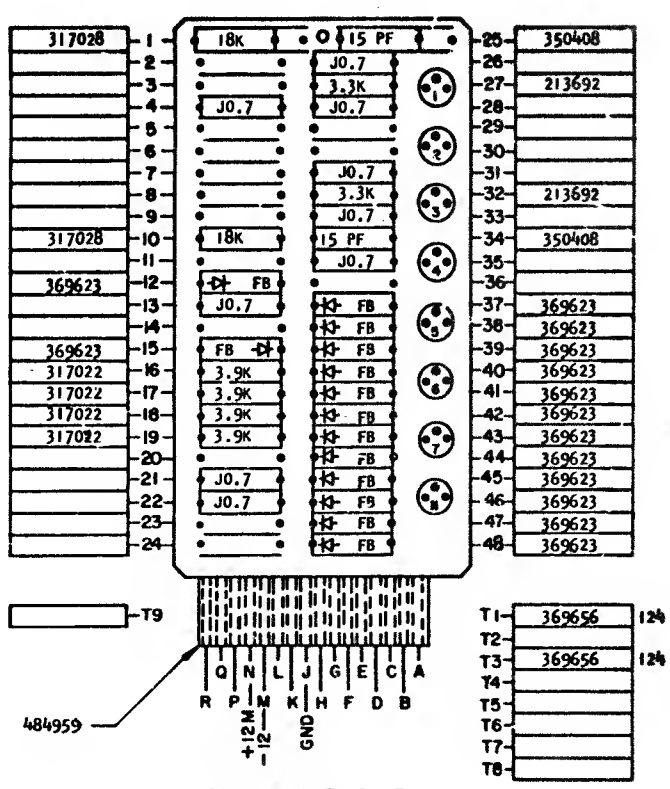
SEQUENCE OF OPERATION

1. PINS L, B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D43.
2. PINS A AND O MUST BE DOWN TO HAVE A DOWN LEVEL AT D44.
3. EITHER LEVEL DOWN AT D43 OR D44 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT TO BE UP.
4. EITHER L OR B OR C UP WILL CAUSE AN UP LEVEL AT D43.
5. EITHER O OR A UP WILL CAUSE AN UP LEVEL AT D44.
6. BOTH LEVELS AT D43 AND D44 MUST BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	15	280
TURN OFF (NSEC)	24	300



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL HS 1 2-WAY, 1 3-WAY NEG AND- NEG OR LOGIC BLOCKS W/O LOADS					4-25-63	116800B					
DESIGN			MODEL	SMS 1460								
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE	2-8-63							
APPRO	WCG	4-25-63	CHECK									

734381

734375

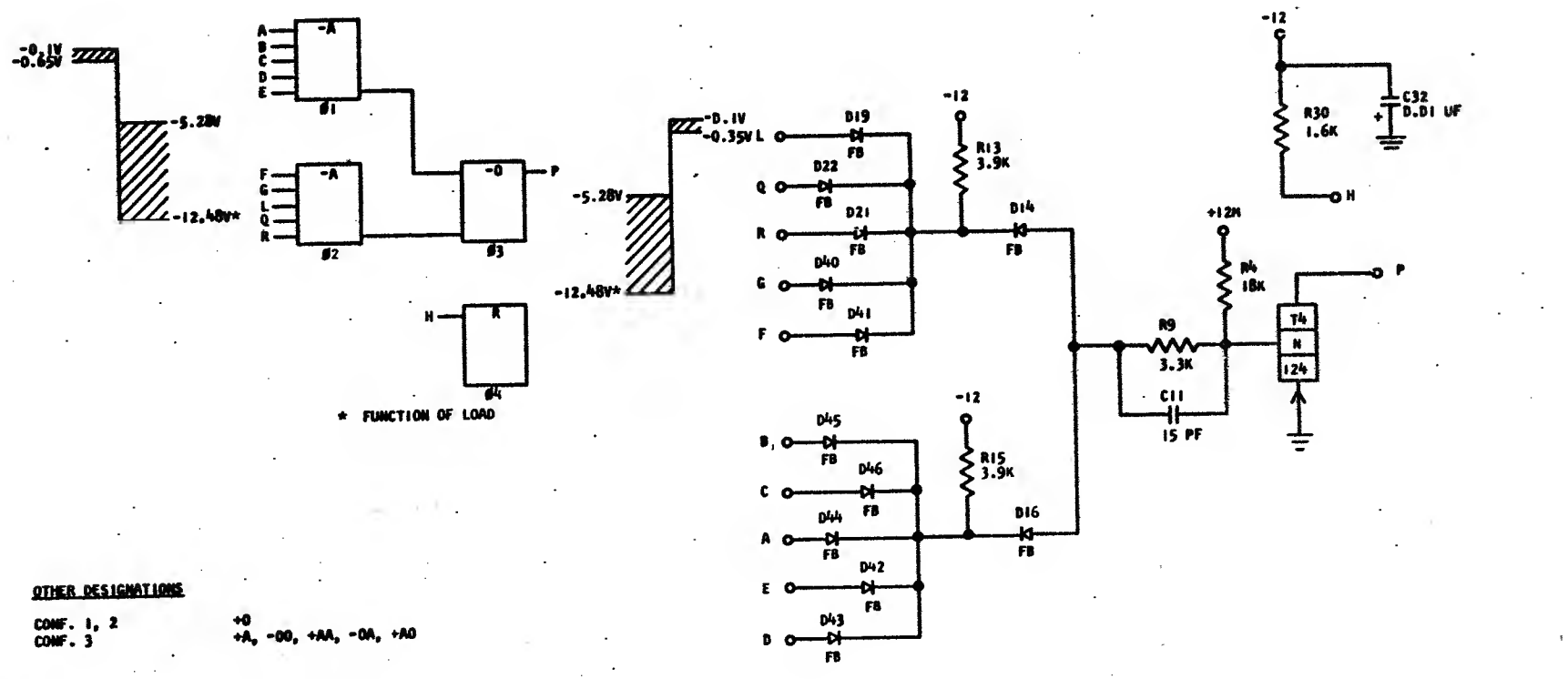
734375

CEZ-

P/N: 372525 EC: 0116156

REFERENCE DRAWING
PRODUCTION DRAWING 372525

SDTDL HS TWO 5-WAY NEGATIVE AND - NEGATIVE OR LOGIC BLOCKS WITH OR WITHOUT LOADS



★ FUNCTION OF LOAD

OTHER DESIGNATIONS

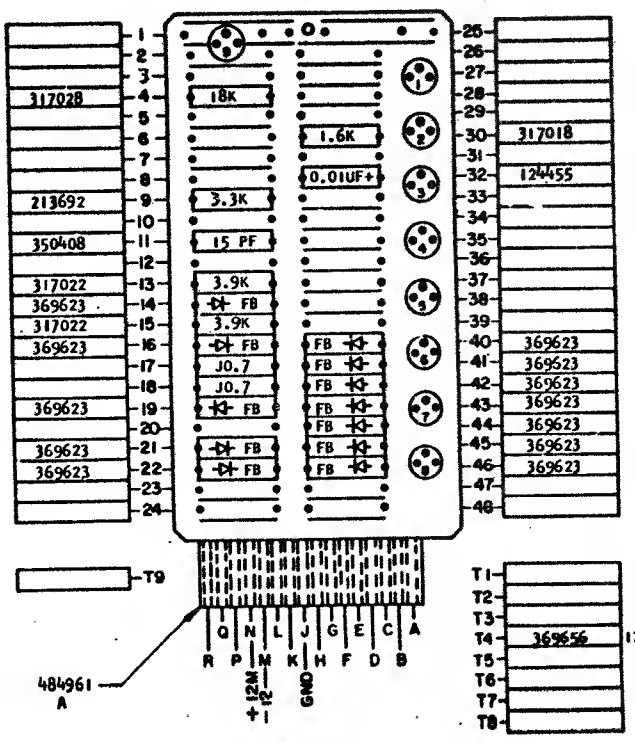
CONF. 1, 2	+0
CONF. 3	+A, -00, +AA, -0A, +A0

SEQUENCE OF OPERATION

1. PINS A, B, C, D AND E MUST BE DOWN TO HAVE A DOWN LEVEL AT D16.
2. PINS F, G, L, Q AND R MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
3. A DOWN LEVEL AT D14 OR D16 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER A, B, C, D OR E UP WILL CAUSE AN UP LEVEL AT D16.
5. EITHER F, G, L, Q OR R UP WILL CAUSE AN UP LEVEL AT D14.
6. THE LEVELS AT D14 AND D16 MUST BOTH BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	15	280
TURN OFF (NSEC)	24	300



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734375
NAME	SDTDL HS TWO 5-WAY NEG AND-NEG OR LOGIC BLOCKS W OR W/O LOADS				4-25-63	1168009						
DESIGN			MODEL	SMS 1460								
DETAIL			SCALE	NONE								
CHECK			DRAW	P.OE 2-8-63								
APPRD	[illegible] 4-25-63		CHECK									

C

STANDARDS CODE 2-7045

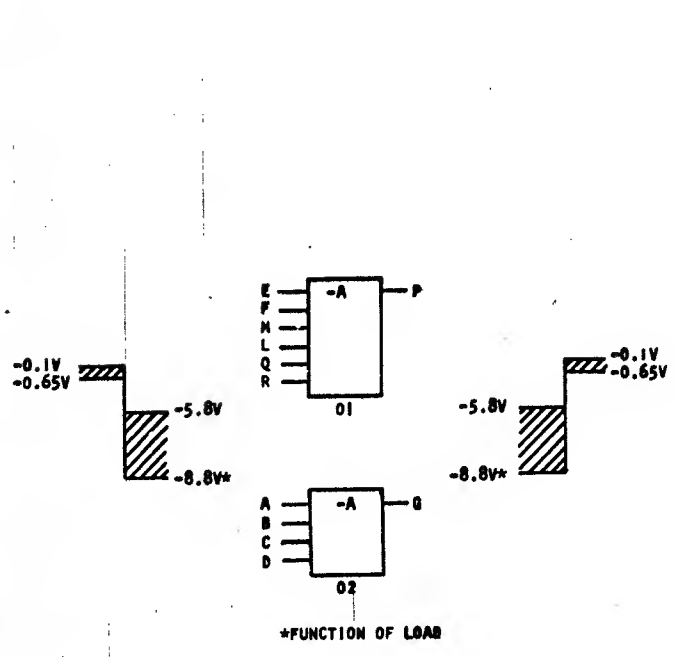
734304

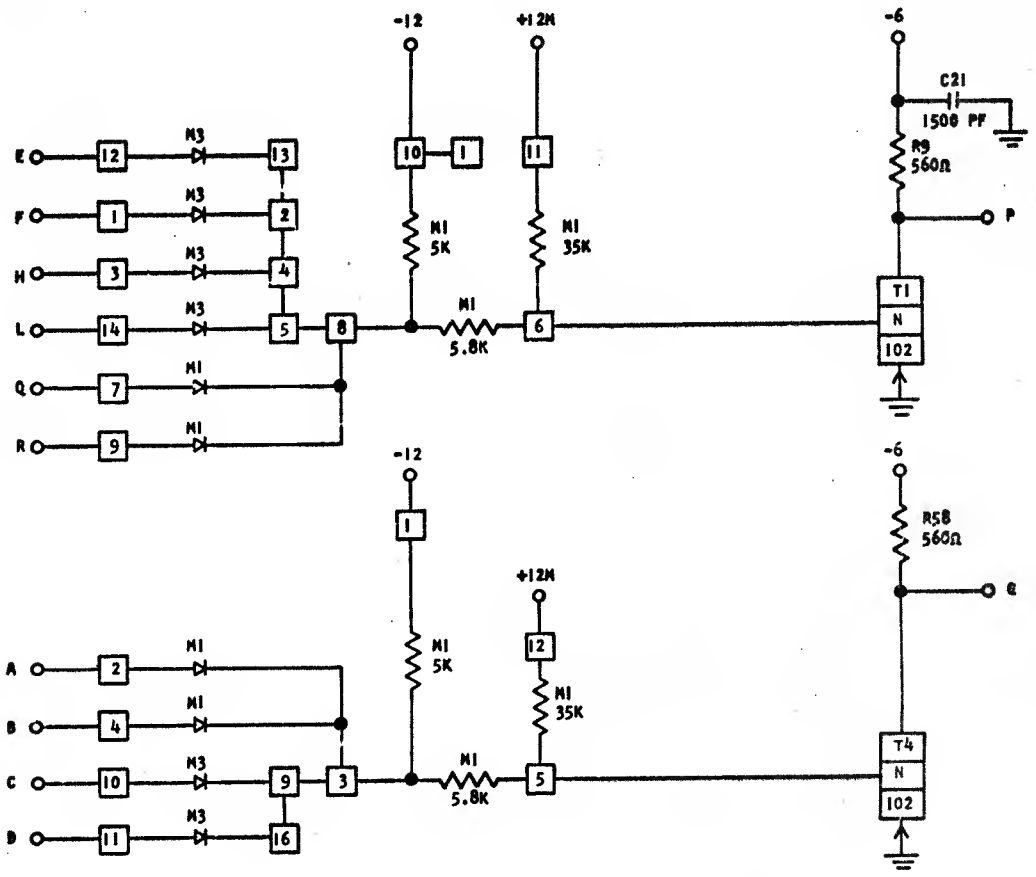
CARD CODE 734304

DEN -

REFERENCE DRAWING
SEE PRODUCTION DRAWING 372195

1 6-WAY, 1 4-WAY NEGATIVE AND LOGIC BLOCKS WITH LOADS





OTHER DESIGNATIONS:

+0, +A0, +0A, +00, I, ID, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

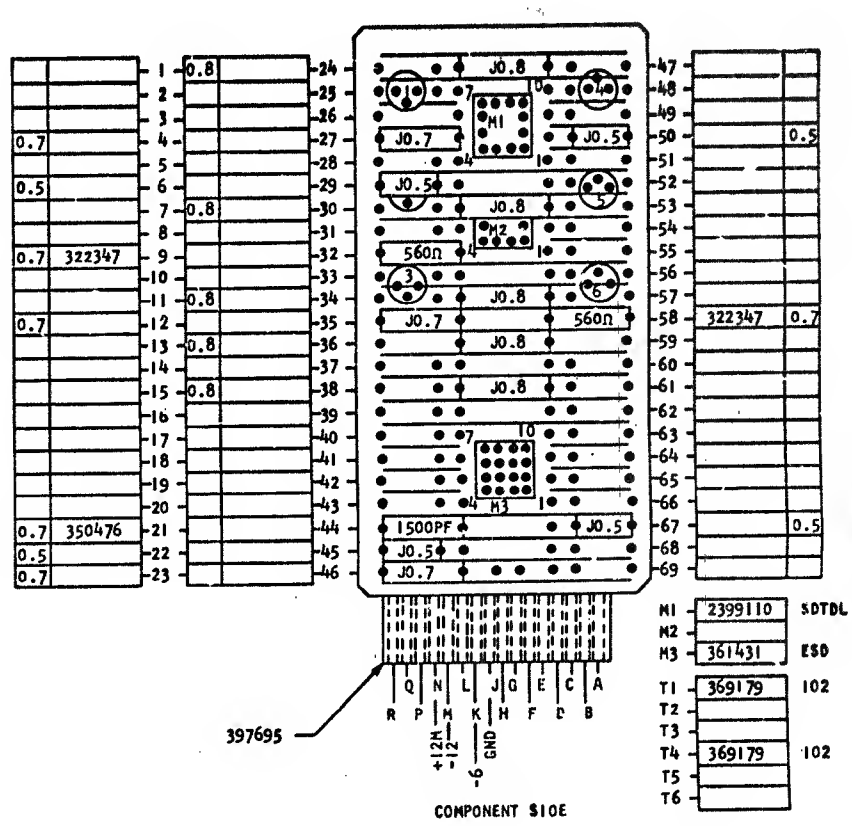
DELAY

	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	LS 1 6-WAY, 1 4-WAY NEG. AND LOGIC BLOCKS WITH LOADS				
DESIGN			MODEL	SMS	
DETAIL			SCALE	NONE	
CHECK			DRAW	LIG	20OCT67
APPRO			CHECK	JD	26OCT67

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
25MAR63	116800					
30DEC63	119217					
12 FEB 68	132166					
						CIRCUIT FAMILY
						SDTDL

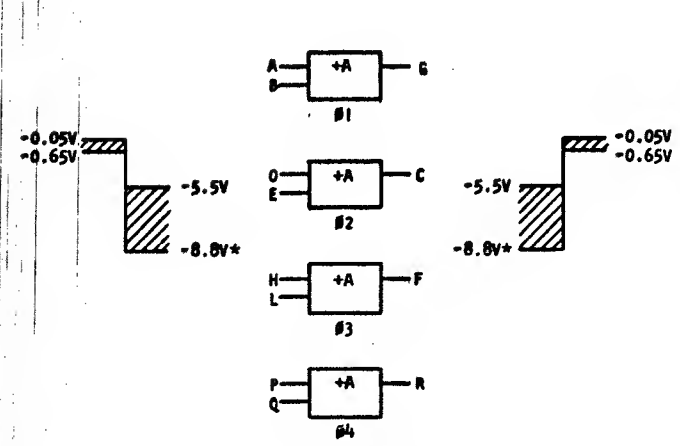
734304

C

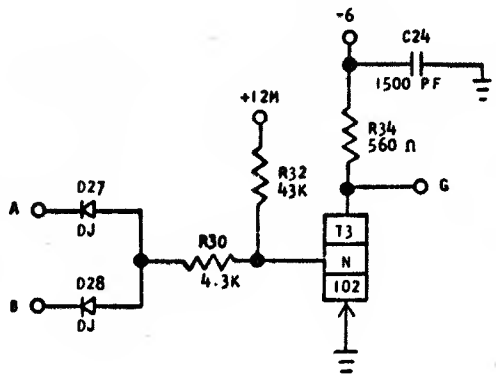
DIETZGEN PRESS, INC. BROOKLYN 17, N.Y. STOCK NO. 6907

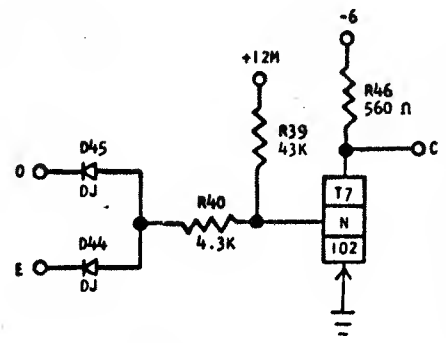
REFERENCE DRAWING
PRODUCTION DRAWING 372196

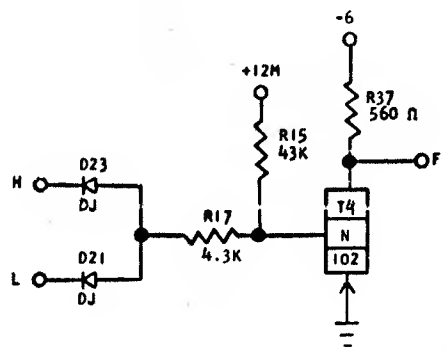
SDTDL LS 4 2-WAY POSITIVE AND LOGIC BLOCKS WITH LOADS

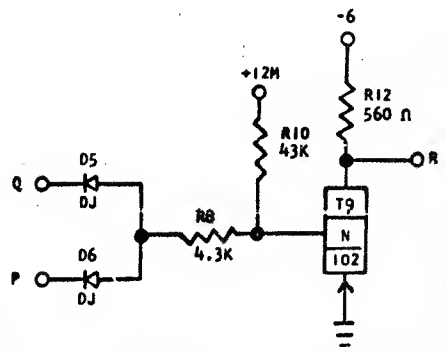


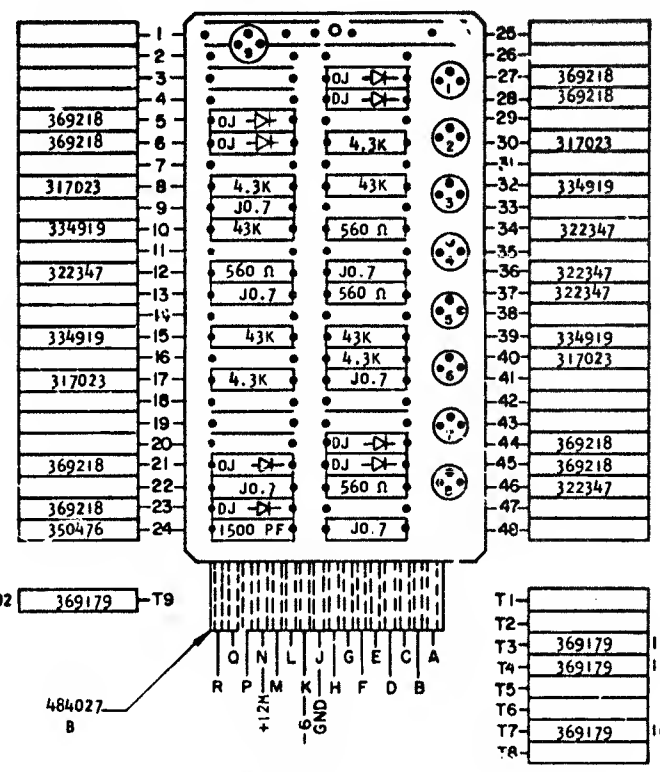
* FUNCTION OF LOAD











COMPONENT SIDE

OTHER DESIGNATIONS:

-0, +A0, -0A, +AA, -00

SEQUENCE OF OPERATION

1. ALL INPUTS UP: TRANSISTOR OFF, OUTPUT DOWN.
2. ANY INPUT DOWN: TRANSISTOR ON, OUTPUT UP.

DELAY

	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
-N.A.F.	20FEB62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	SDTDL LS 4 2-WAY POS AND LOGIC BLOCKS WITH LOADS				
DESIGN		MODEL	SMS		
DETAIL		SCALE	NONE		
CHECK		DRAW	MDE	12-10-62	
APPRO		CHECK			

DATE	CHANGE NO.	APPROVAL
3-25-63	116800	
10-21-63	118933	
100EC55	126162	GLK
23FEB66	127160	GLK

DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.

734305

2-0

STANDARDS CODE 729909

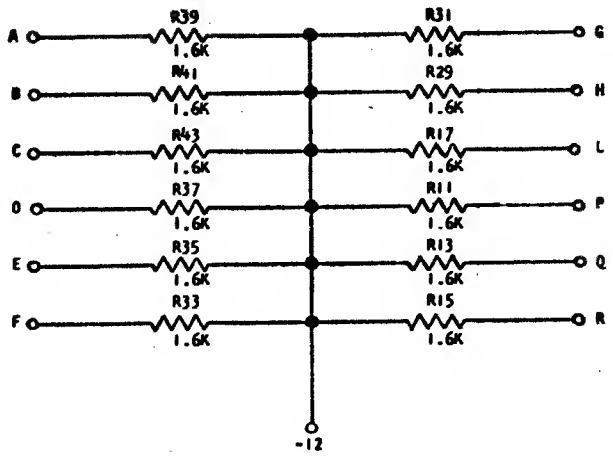
CARD CODE 729909

D F J -

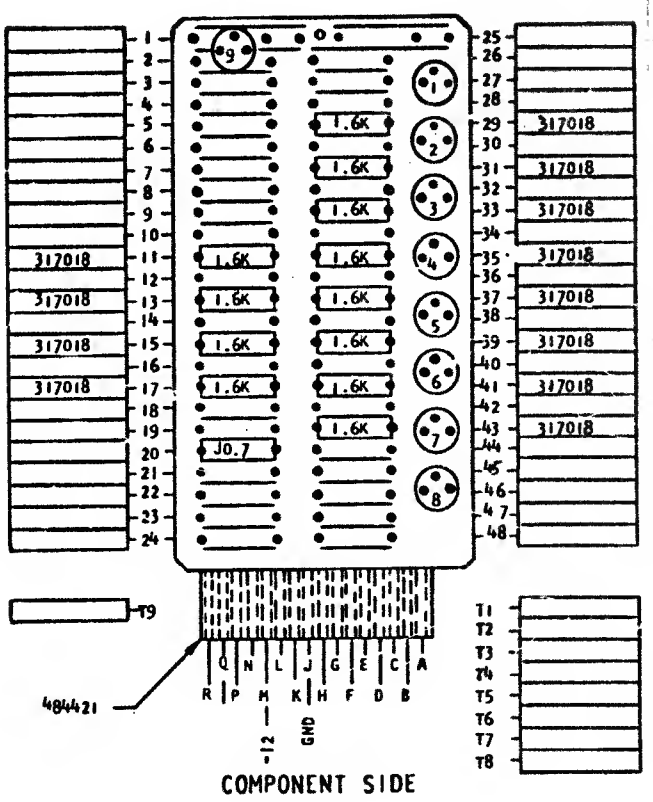
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370232

TDL & TRL LOAD CARD



APPLICATION
1. USED FOR TDL AND TRL COLLECTOR LOADING
2. MAY BE USED IN PARALLEL IN CERTAIN APPLICATIONS



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-TDL AND TRL LOAD CARD				6-29-62	115599					
					7-30-63	117824					
DESIGN			MODEL	SMS 8018							
DETAIL	RQ	2-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	JRP 7-11-63							
APPRO			CHECK	7-12-63							

729909

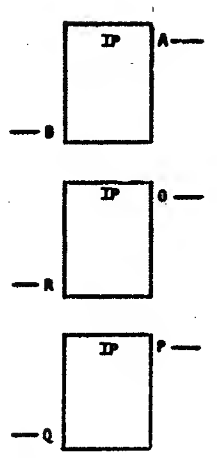
2-0

STANDARDS CODE	
2-7045	729910

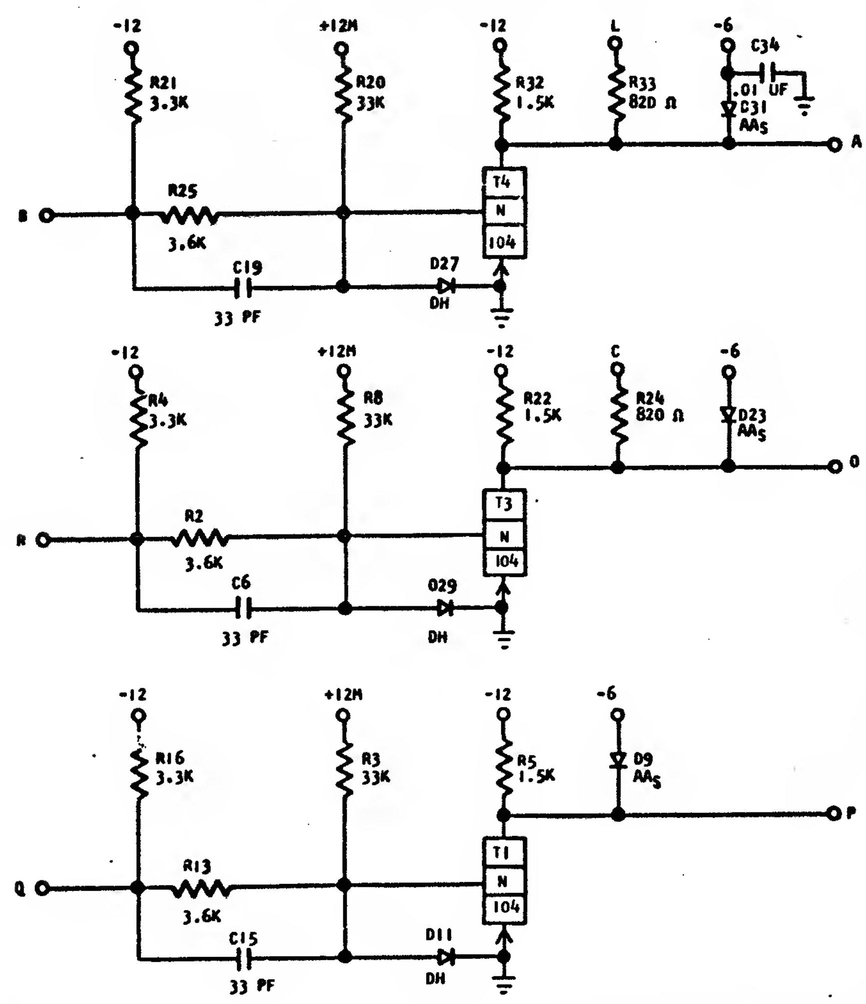
CARD CODE	729910
D F Q -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370225



INVERTING POWER DRIVER



SEQUENCE OF OPERATION

1. INPUT DOWN, TRANSISTOR ON, OUTPUT UP.
2. INPUT UP, TRANSISTOR OFF, OUTPUT DOWN.
3. 820Ω COLLECTOR RESISTOR RETURNED TO -12 VOLTS WHEN DRIVING NEGATIVE "OR" INPUTS OF DOUBLE LEVEL LOGIC BLOCKS AND WHEN DRIVING TRIGGER AC INPUTS.

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
B,R,Q	Y	INPUT		UP	-0.65	-0.10
				DOWN	-7.14	-5.84
A,O,P	Y	OUTPUT		UP	-0.65	-0.10
				DOWN	-6.06	-6.8

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	10.0**	50.0*
TURN OFF	14.0**	35.0*

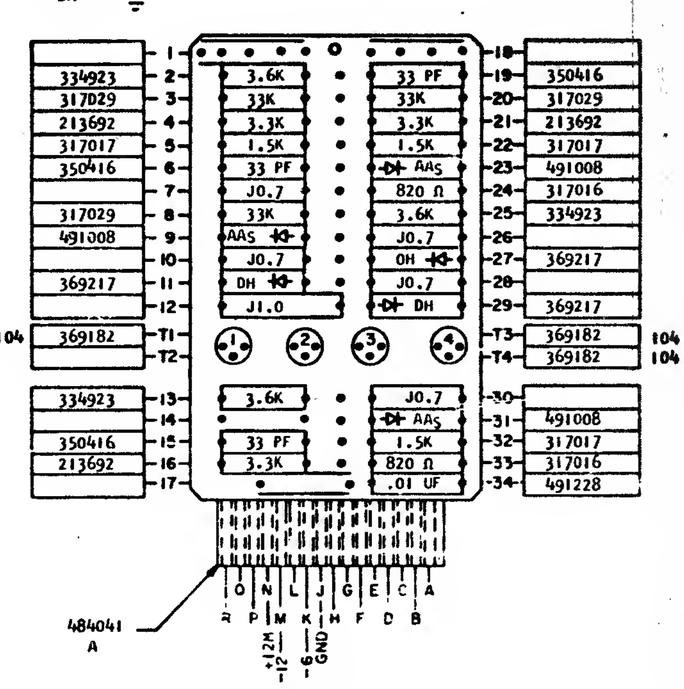
*ASSUMES LOAD OF 10 LOGIC BLOCKS AND TR INPUT OF 70 NSEC AND INPUT TF OF 135 NSEC.

**ASSUMES LOAD OF 4 LOGIC BLOCKS AND INPUT TR OF 35 NSEC AND INPUT TF OF 70 NSEC.

RISE TIME	16.0	70.0# TO 110.0##
FALL TIME	75.0	125.0## TO 190.0#

#OCCURS WHEN DRIVING TRIGGERS.

##OCCURS WHEN DRIVING LOGIC BLOCKS.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASSEMBLY TRANSISTOR - INVERTING POWER DRIVER				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6-29-62	115599					
12-30-63	119217					
						CIRCUIT FAMILY
						SDTDL

729910

C

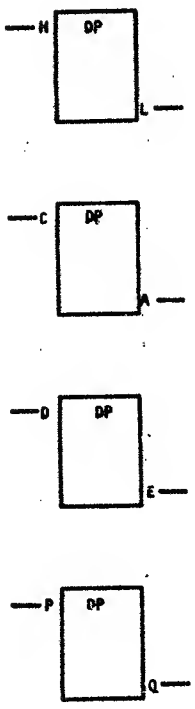
729911 | STANDARDS CODE

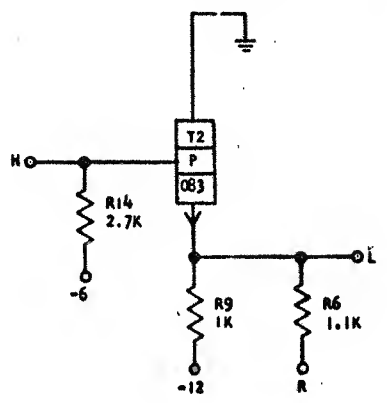
CARD CODE 729911
D F R -

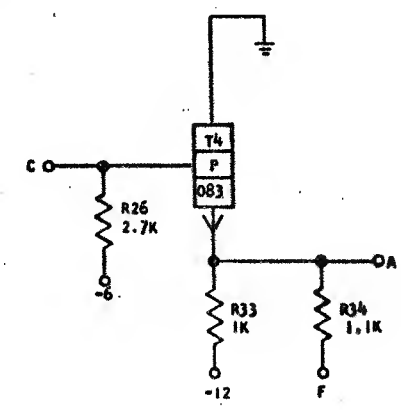
REFERENCE DRAWING

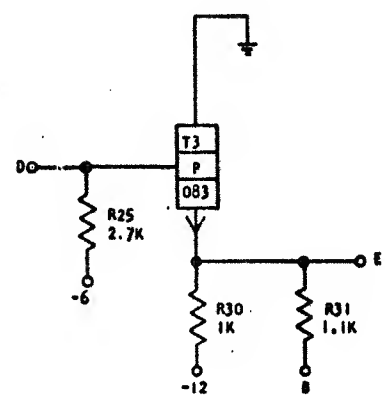
SEE PRODUCTION DRAWING 370226

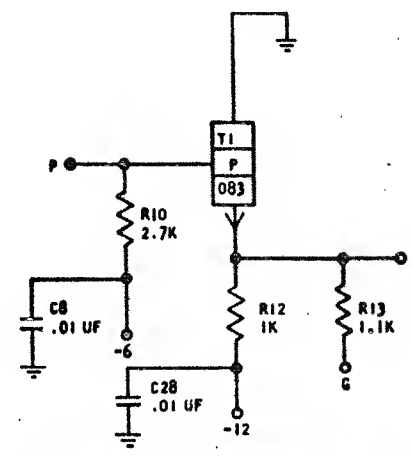
SDTDL NON-INVERTING POWER DRIVER











SEQUENCE OF OPERATION

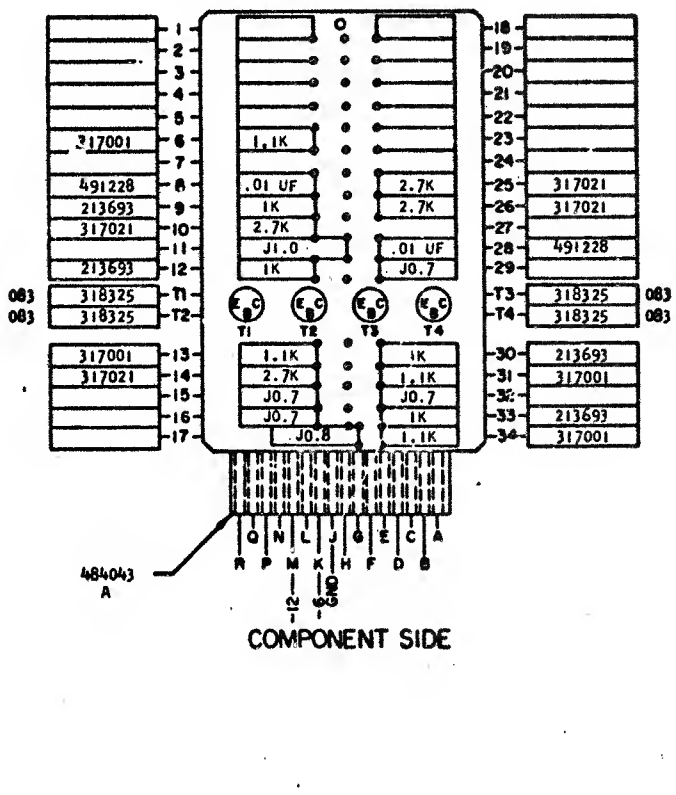
1. OUTPUT WILL FOLLOW INPUT
2. PINS R, F, B, AND G MAY BE CONNECTED TO PIN M (-12) FOR CERTAIN APPLICATIONS.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
H,C, D,P	Y	INPUT		UP	-0.65	-0.10
				DOWN	-5.81	-8.8
L,A, E,Q	Y	OUTPUT		UP	-1.10	-0.22
				DOWN	-7.30	-5.83

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	6.0	20.0
TURN OFF	6.0	28.0

OUTPUT RISE AND FALL TIMES ARE WITHIN ±10 NSEC'S OF THE INPUT RISE AND FALL TIMES, RESPECTIVELY.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD

APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL NON-INVERTING POWER DRIVER					6-29-62	115599					
DESIGN			MODEL	SMS		1-3-63	116034					
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729911

C

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734348

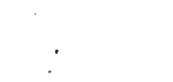
734348

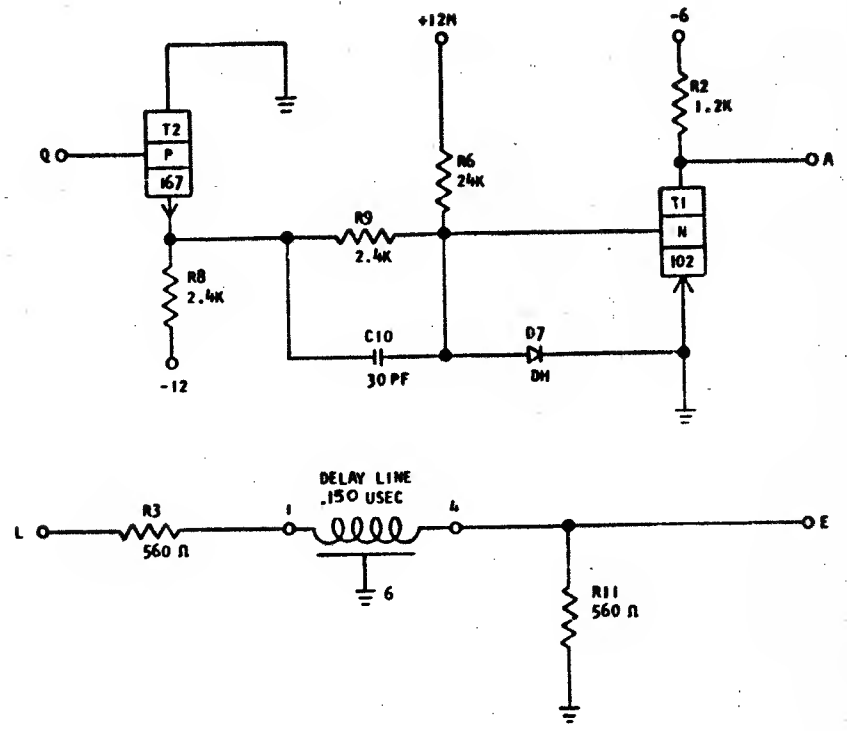
DGC—

P/N: 370244

REFERENCE DRAWING
PRODUCTION DRAWING 370244

SDTDL MEMORY .15D USEC DELAY LINE





SEQUENCE OF OPERATION

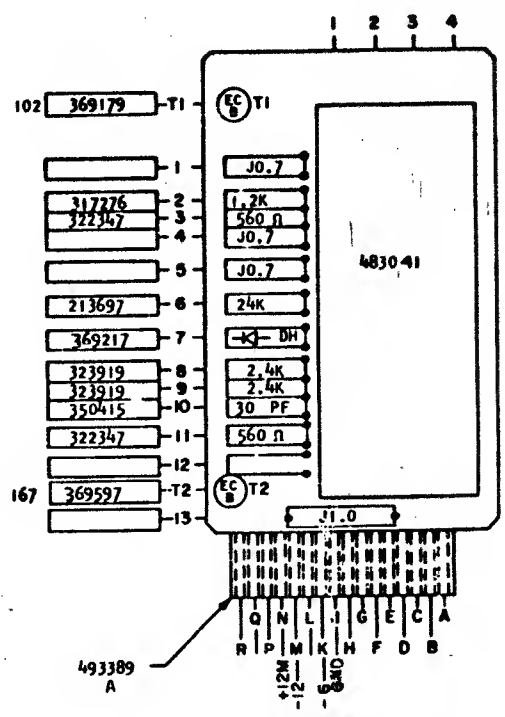
1. INPUT UP: TRANSISTOR (T_2) ON, TRANSISTOR (T_1) OFF, OUTPUT DOWN.
2. INPUT DOWN: TRANSISTOP (T_2) OFF, TRANSISTOR (T_1) ON, OUTPUT UP.

PINS	SIGNAL NAME		WAVESHAPE		LEVELS MIN	LEVELS MAX
L	Y	INPUT		UP	-.65V	-.1V
				DOWN	-6.06V	-7.04V
Q	Y	INPUT		UP	-.39V	0.0V
				DOWN	-2.66V	-3.54V
A	Y	OUTPUT		UP	-.65V	-.1V
				DOWN	-5.81V*	-6.76V

* DOWN LEVEL IS A FUNCTION OF LOAD

DELAY THRU DT - (PIN Q TO PIN A)

	MIN	NOM	MAX
T_{ON} (NSEC)	50	60	70
T_{OFF} (NSEC)	55	68	80



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	SOTOL MEMORY .150 USEC DELAY LINE				
DESIGN			MODEL	SMS 1440	
DETAIL			SCALE	NONE	
CHECK			DRAW	MOE	1-9-63
APPRD		4-17-63	CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
4-17-63	116800A					
1-25-65	123184					
14OCT65	125832					

734348

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734349

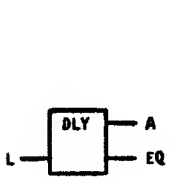
734349

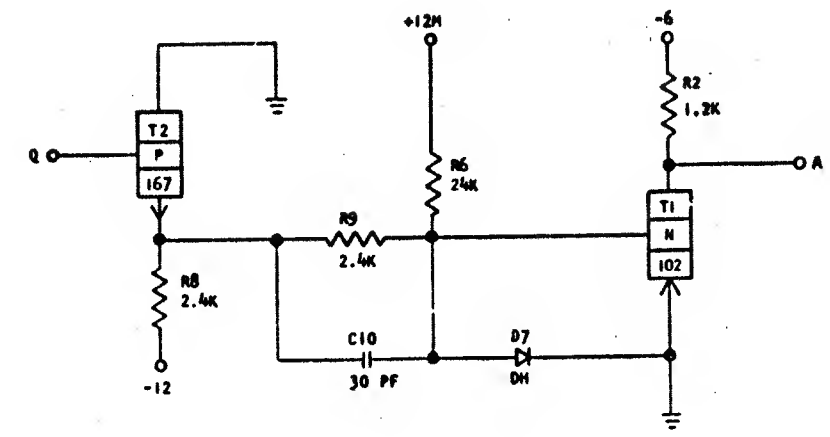
DGD—

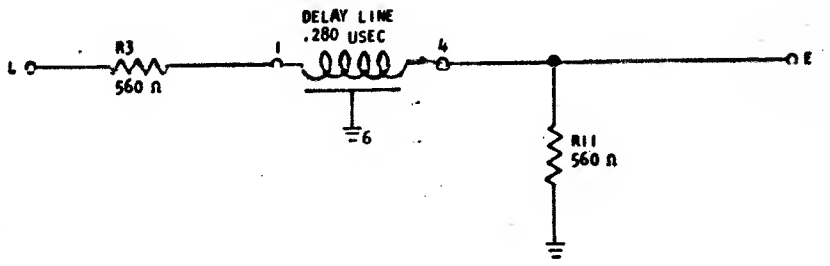
P/N: 370245

REFERENCE DRAWING
PRODUCTION DRAWING 370245

SDTDL MEMORY .280 USEC DELAY LINE







SEQUENCE OF OPERATION

1. INPUT UP: TRANSISTOR (T_2) ON, TRANSISTOR (T_1) OFF, OUTPUT DOWN.
2. INPUT DOWN: TRANSISTOR (T_2) OFF, TRANSISTOR (T_1) ON, OUTPUT UP.

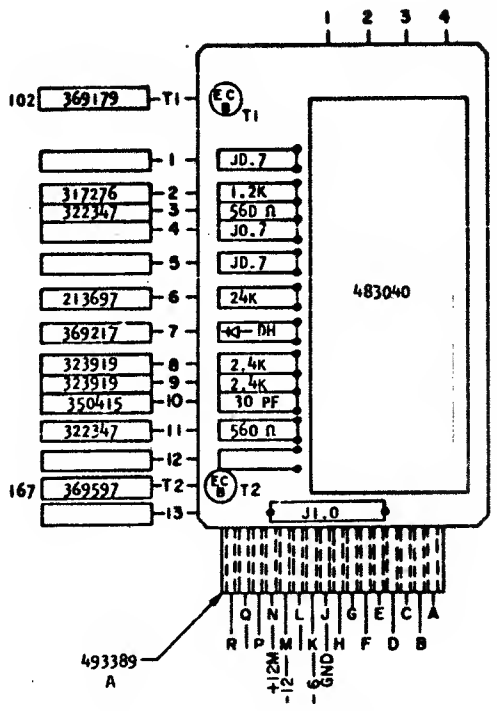
PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
L	Y	INPUT		UP	-.65V	-.1
				DOWN	-6.06V	-7.04V
Q	Y	INPUT		UP	-.39V	0.0V
				DOWN	-2.66V	-3.54V
A	Y	OUTPUT		UP	-.65V	-.1V
				DOWN	-5.81V*	-6.76V

.280 USEC .280 USEC

* DOWN LEVEL IS A FUNCTION OF LOAD

DELAY THRU DT - (PIN Q TO PIN A)

	MIN	NOM	MAX
T_{ON} (NSEC)	50	60	70
T_{OFF} (NSEC)	55	68	80



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	SDTDL MEMORY .280 USEC DELAY LINE				
DESIGN			MODEL	SMS 1440	
DETAIL			SCALE	NONE	
CHECK			DRAW	MDE	1-9-63
APPRD		3-25-63	CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
3-25-63	116800					
140CT65	125832					

734349

FORM 46-001

2-0

734351

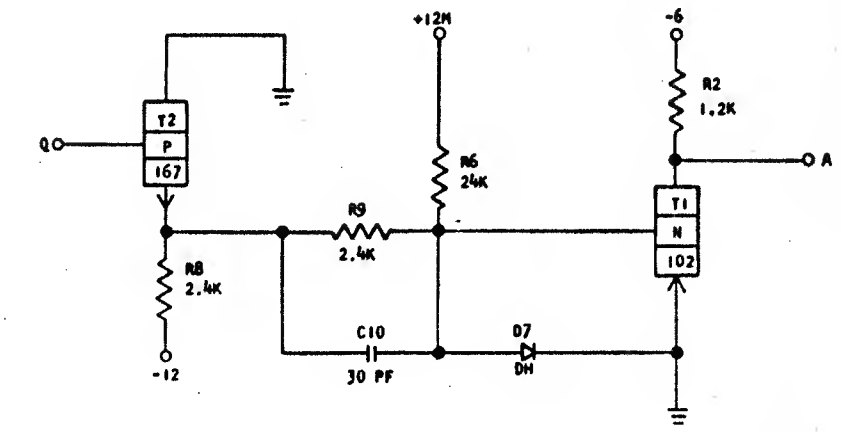
734351

DGF—

P/N: 370247

REFERENCE DRAWING
PRODUCTION DRAWING 370247

SDTDL MEMORY .525 USEC DELAY LINE



SEQUENCE OF OPERATION

1. INPUT UP: TRANSISTOR (T_2) ON, TRANSISTOR (T_1) OFF, OUTPUT DOWN.
2. INPUT DOWN: TRANSISTOR (T_2) OFF, TRANSISTOR (T_1) ON, OUTPUT UP.

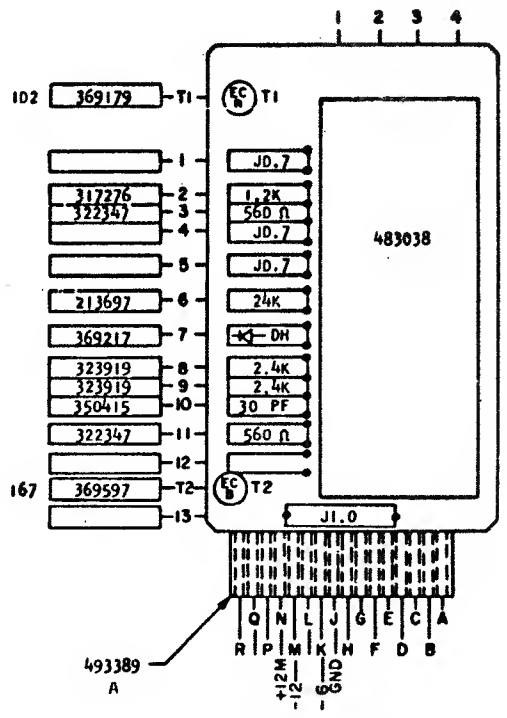
PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
L	Y	INPUT		UP	-.65V	-.1V
				DOWN	-6.06V	-7.04V
Q	Y	INPUT		UP	-.39V	-0.0V
				DOWN	-2.66V	-3.54V
A	Y	OUTPUT		UP	-.65V	-.1V
				DOWN	-5.81*	-6.76V

.525 USEC .525 USEC

* DOWN LEVEL IS A FUNCTION OF LOAD.

DELAY THRU DT - (PIN Q TO PIN A)

	MIN	NOM	MAX
T_{DN} (NSEC)	50	60	70
T_{OFF} (NSEC)	55	68	80



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734351
NAME	SDTDL MEMORY .525 USEC DELAY LINE					3-25-63	116800						
DESIGN			MODEL	SMS 1440		140CT65	125832						
DETAIL			SCALE	NONE									
CHECK			DRAW	MDE	1-9-63								
APPRD	REJ	3-25-63	CHECK										

C

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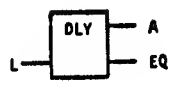
734352

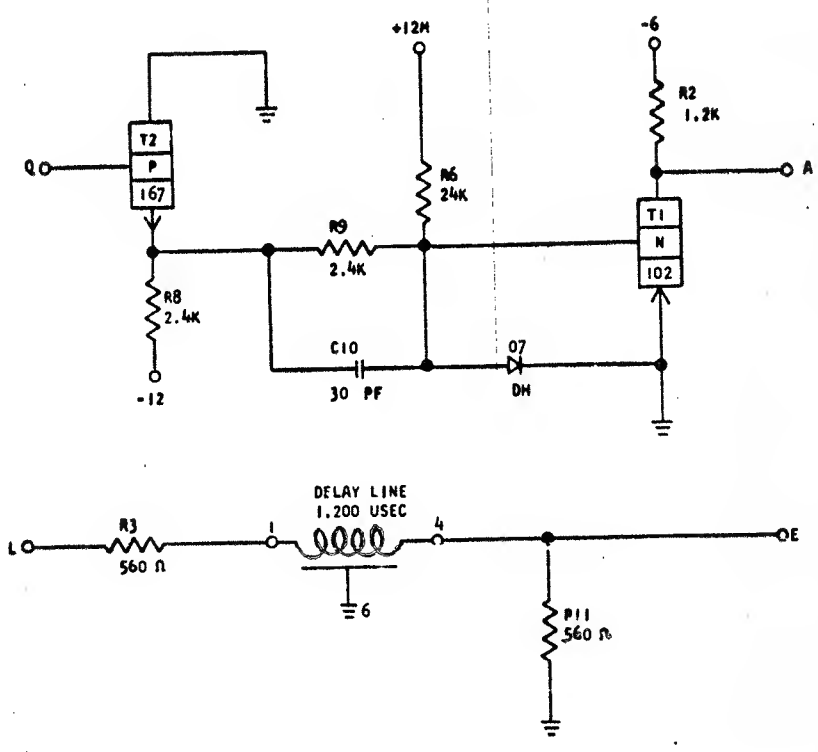
DGH-

P/N: 370249

REFERENCE DRAWING
PRODUCTION DRAWING 370249

SDTDL MEMORY 1.200 USEC DELAY LINE





SEQUENCE OF OPERATION

1. INPUT UP: TRANSISTOR (T_2) ON, TRANSISTOR (T_1) OFF, OUTPUT DOWN.
2. INPUT DOWN: TRANSISTOR (T_2) OFF, TRANSISTOR (T_1) ON, OUTPUT UP.

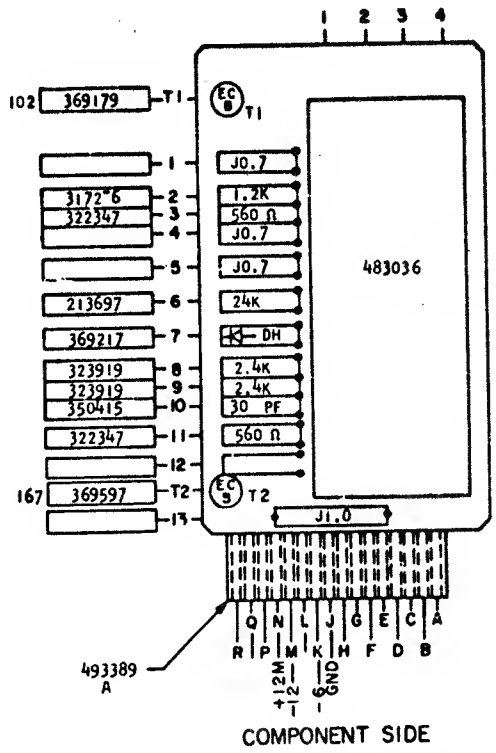
PINS		SIGNAL NAME	WAVESHAPE		LEVELS MIN	LEVELS MAX
L	Y	INPUT		UP	-.65V	-.1V
				DOWN	-6.06V	-7.04V
Q	Y	INPUT		UP	-.39V	-0.0V
				DOWN	-2.66V	-3.54V
A	Y	OUTPUT		UP	-.65V	-.1V
				DOWN	-5.81*	-6.76V

1.200 USEC — 1.200 USEC

* DOWN LEVEL IS A FUNCTION OF LOAD

DELAY THRU DT - (PIN Q TO PIN A)

	MIN	NOM	MAX
T_{ON} (NSEC)	50	60	70
T_{OFF} (NSEC)	55	68	80



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL MEMORY 1.200 USEC DELAY LINE					3-25-63	116800					
						14OCT65	125832					
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE	1-9-63							
APPRD	[illegible]	3-25-63	CHECK									

734352

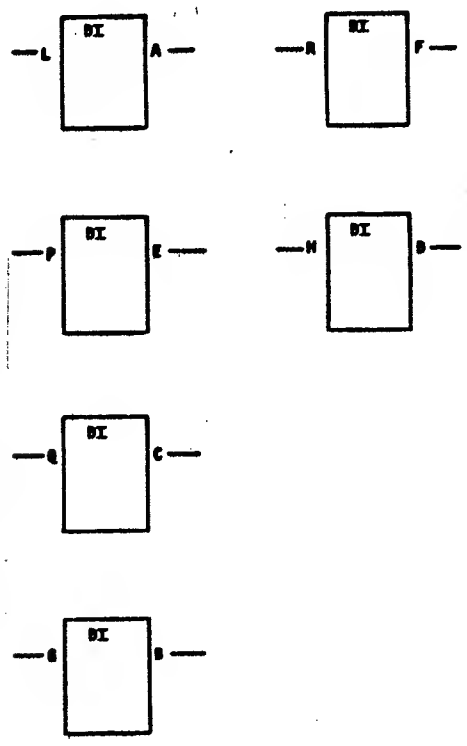
STANDARDS CODE 2-7045

729912

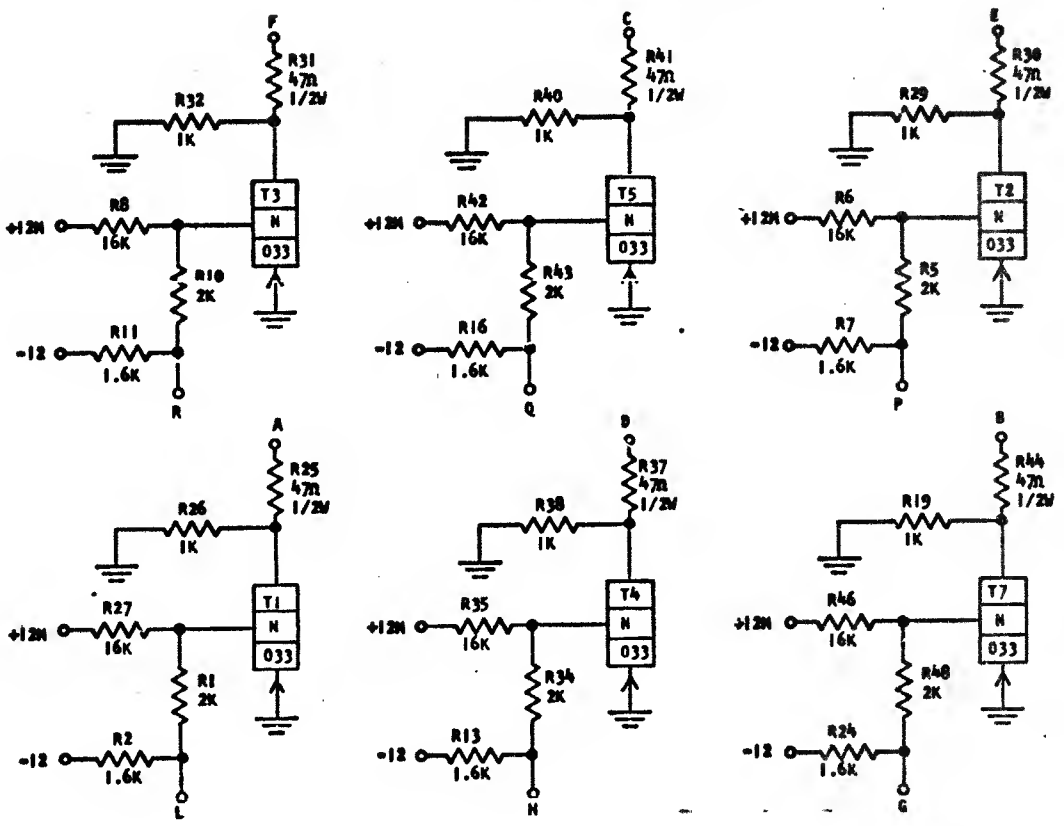
CARD CODE 729912

DGS-

REFERENCE DRAWING
SEE PRODUCTION DRAWING 370347



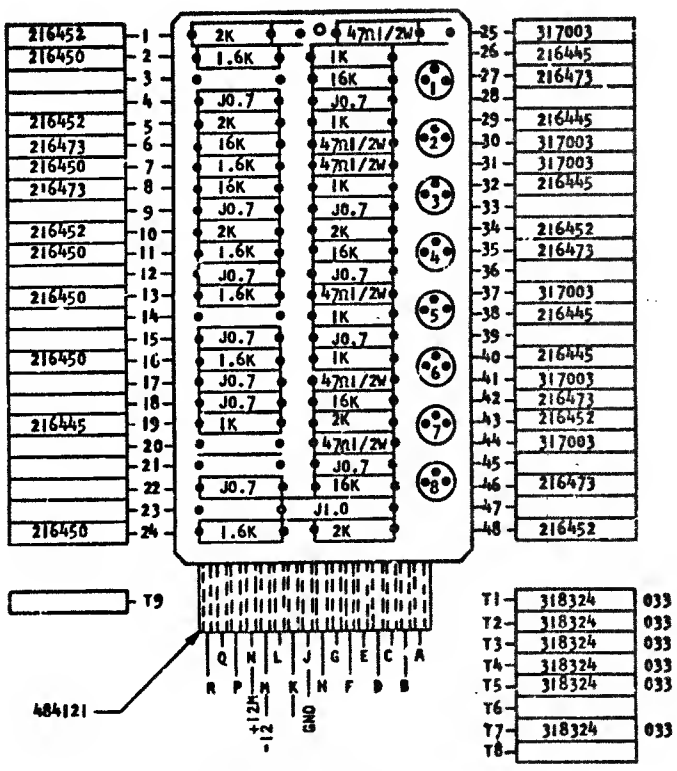
INDICATOR DRIVER



SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
L,R, P,N, Q,G	Y	INPUT		UP	-0.65	0.10
				DOWN	-5.81	-7.64
A,F, E,D, C,B,	S	OUTPUT		UP	-1.67	
				DOWN	-9.62	



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	2APR62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR - INDICATOR DRIVER				
DESIGN			MODEL	SMS	
DETAIL	RQ	1MAR62	SCALE	NONE	
CHECK	WH	1MAR62	DRAW	LIG	8FEB66
APPRO			CHECK	SJ	14FEB66

DATE	CHANGE NO.	APPROVAL
	SEE INDEX CARD	
1MAR63	116026	
1FEB64	119685	
18FEB 66	126401-4	

DATE	CHANGE NO.	APPROVAL

DEVELOPMENT NO.	729912
CIRCUIT FAMILY	
SDTRL	

C

2-0 -1

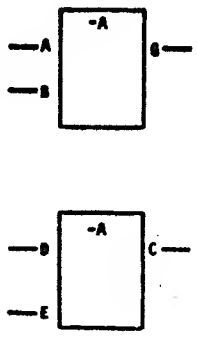
729913 STANDARDS CODE

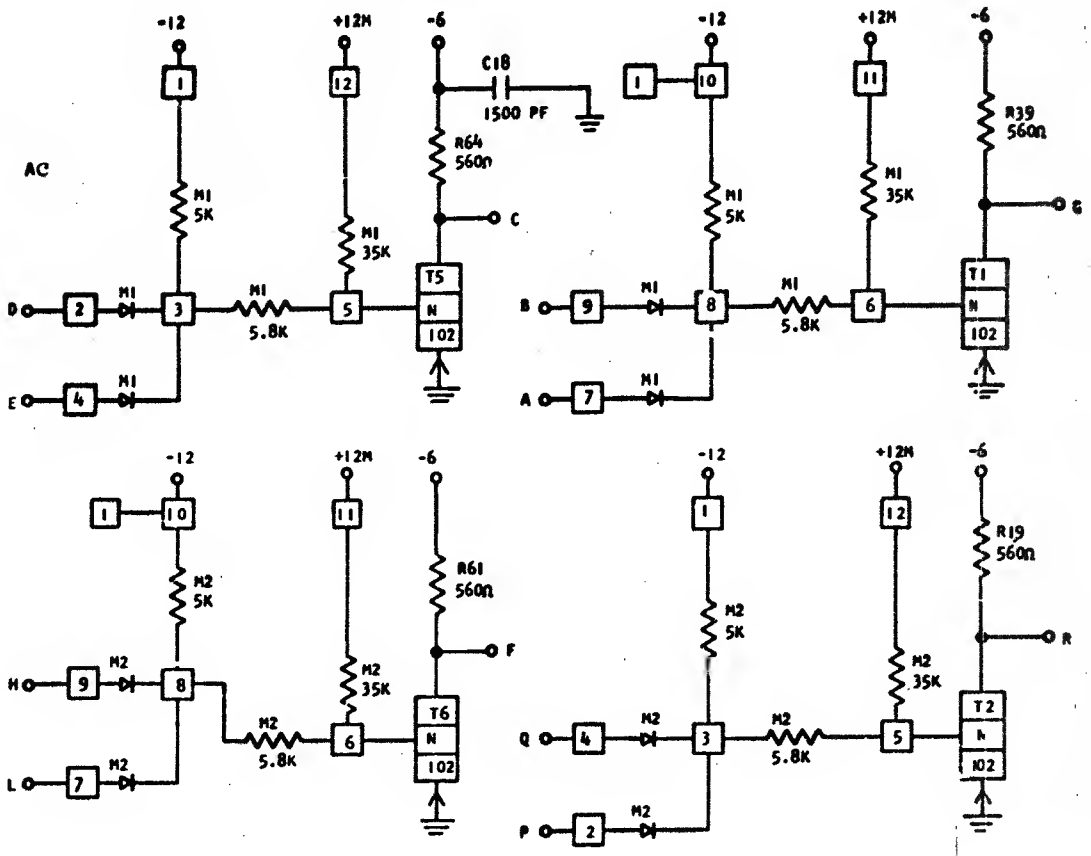
CARD CODE D G T - 729913

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370380

2-WAY LOGIC BLOCK LOW SPEED WITH LOADS

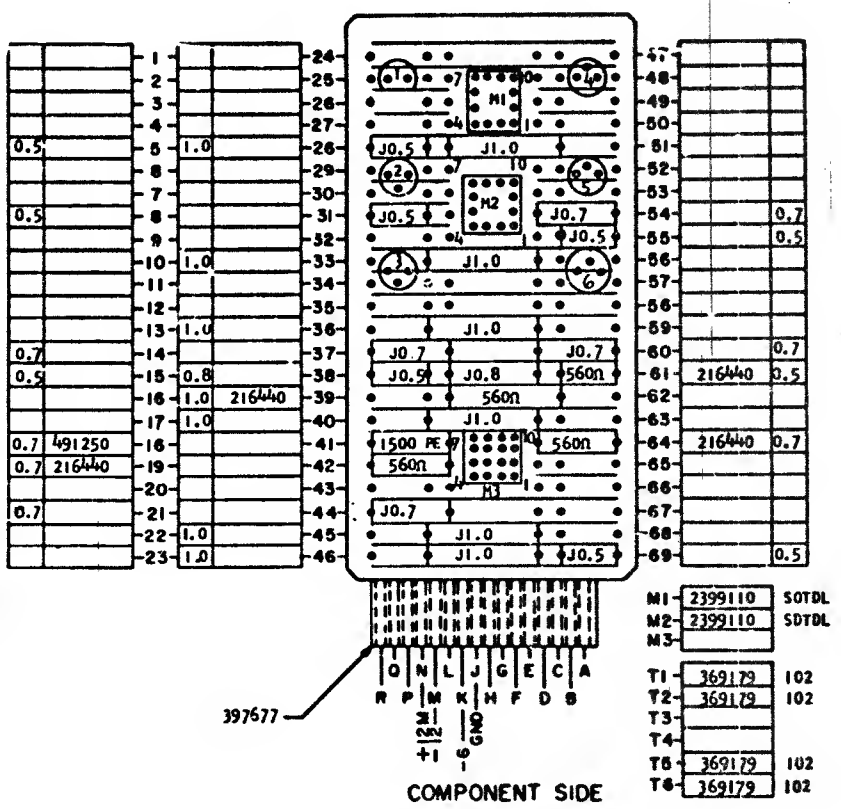




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,D, H,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,E, L,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,C, F,R	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR-SOTOL-2-WAY					6-29-62	115599						729913
	LOGIC BLOCK LOW SPEED WITH LOADS					3-19-63	116153						
DESIGN			MODEL	SMS		10-21-63	118933						
DETAIL	RQ	3-1-62	SCALE	NONE		10DEC65	126162	GLK					
CHECK	WH	3-1-62	DRAW	LIG	3-17-62		132164						
APPRO			CHTCK										

C

2-0

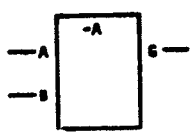
STANDARDS CODE	
729914	

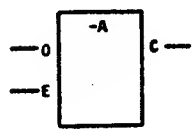
CARD CODE	729914
D G U -	

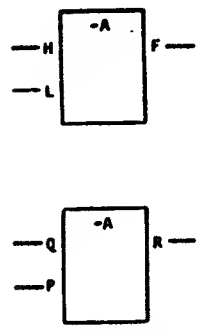
REFERENCE DRAWING

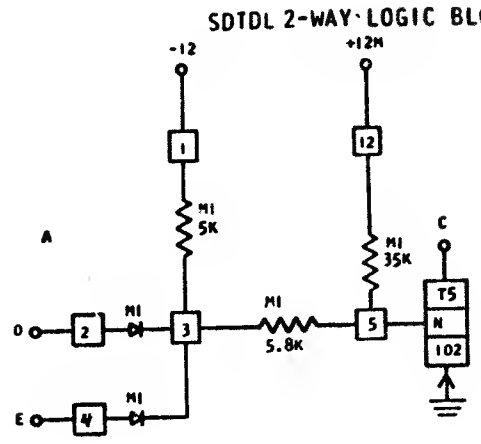
SEE PRODUCTION DRAWING 370379

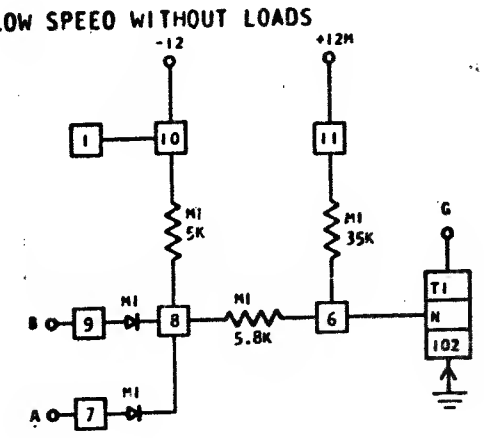
SDTDL 2-WAY LOGIC BLOCK LOW SPEED WITHOUT LOADS

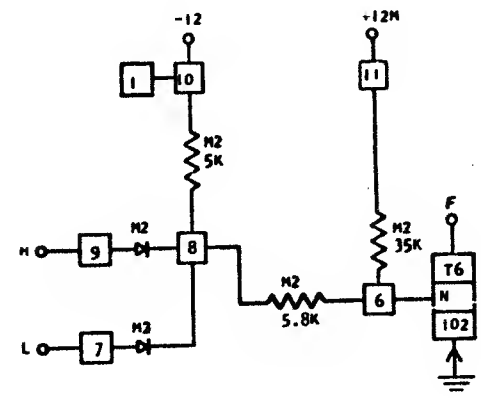


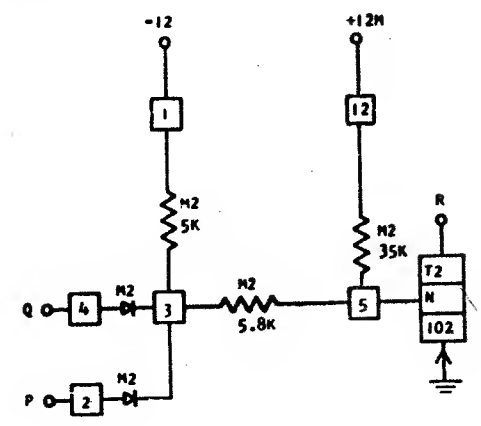










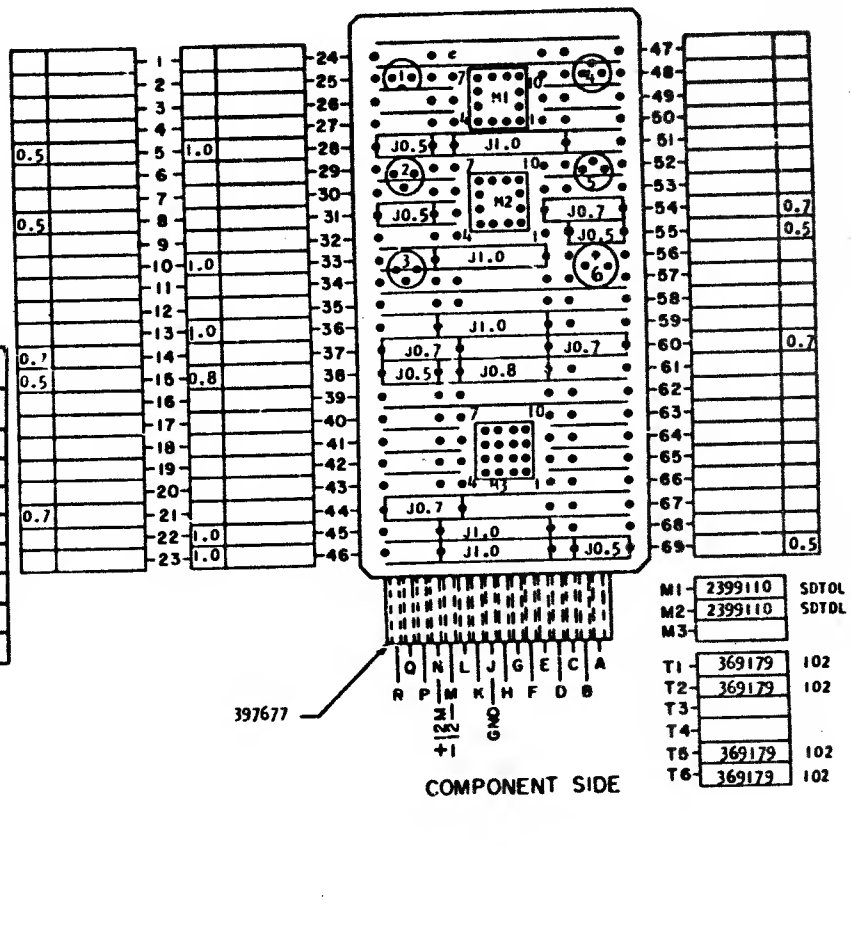


SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT DOWN TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,D, H,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,E, L,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C,G, F,R	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100
TURN OFF (NSEC)	40	200*

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SOTOL 2-WAY LOGIC BCK LOW SPEED WITHOUT LOADS					2-27-62	115599					729914
DESIGN			MODEL	SMS		1-3-63	116034					
DETAIL	RQ	3-1-62	SCALE	NONE		10-21-63	118933					
CHECK	WH	3-1-62	DRAW	LIG	3-17-62	10DEC65	126162	GLK				
APPRO			CHECK			12FEB68	132163					

C

729915

STANDARDS CODE 2-6111

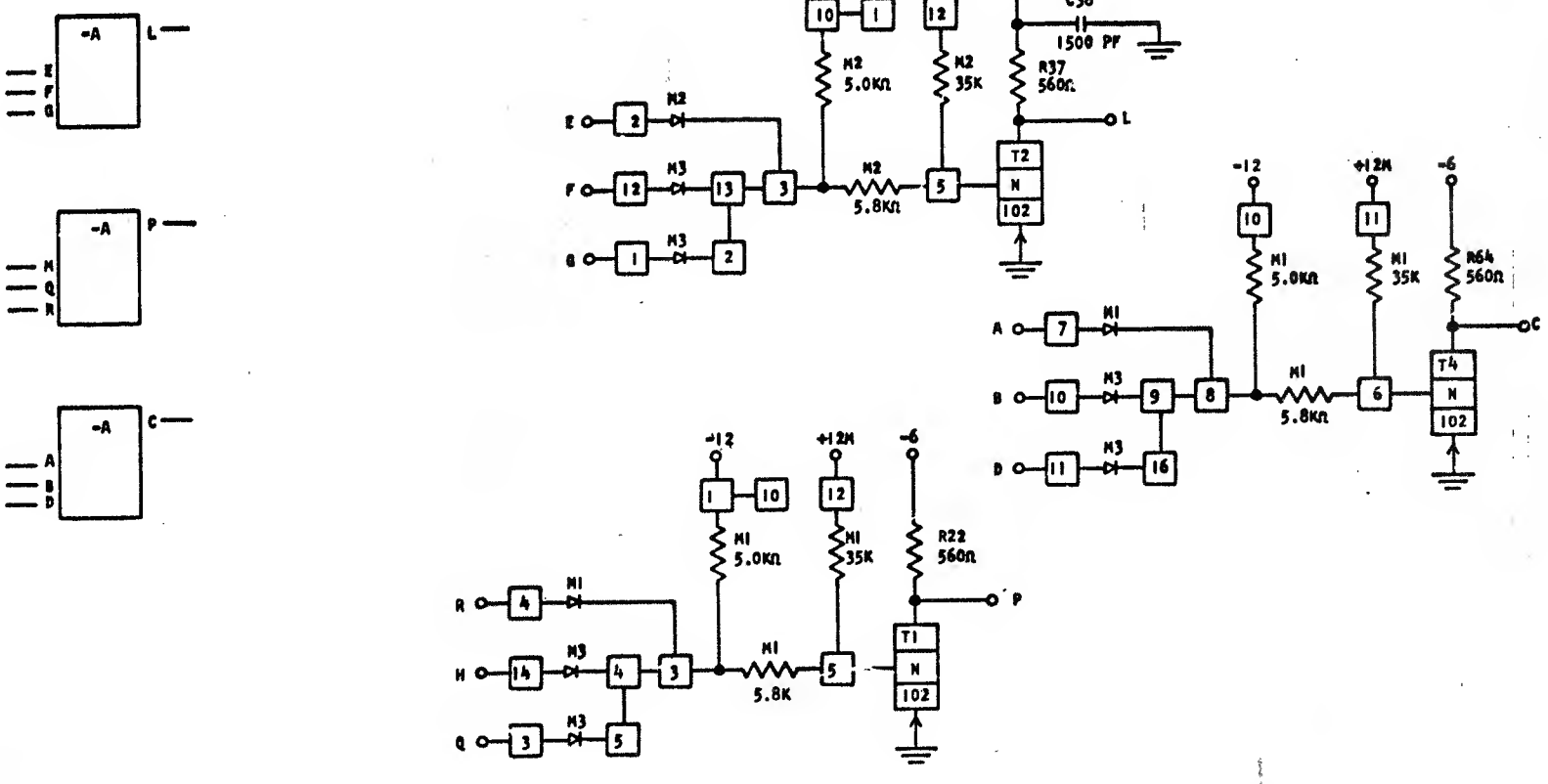
CARD CODE 729915

D G V -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370378

STDTL 3-WAY LOGIC BLOCK LOW SPEED WITH LOADS



SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
E,H, A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F,Q, B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,R, D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L,P, C	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

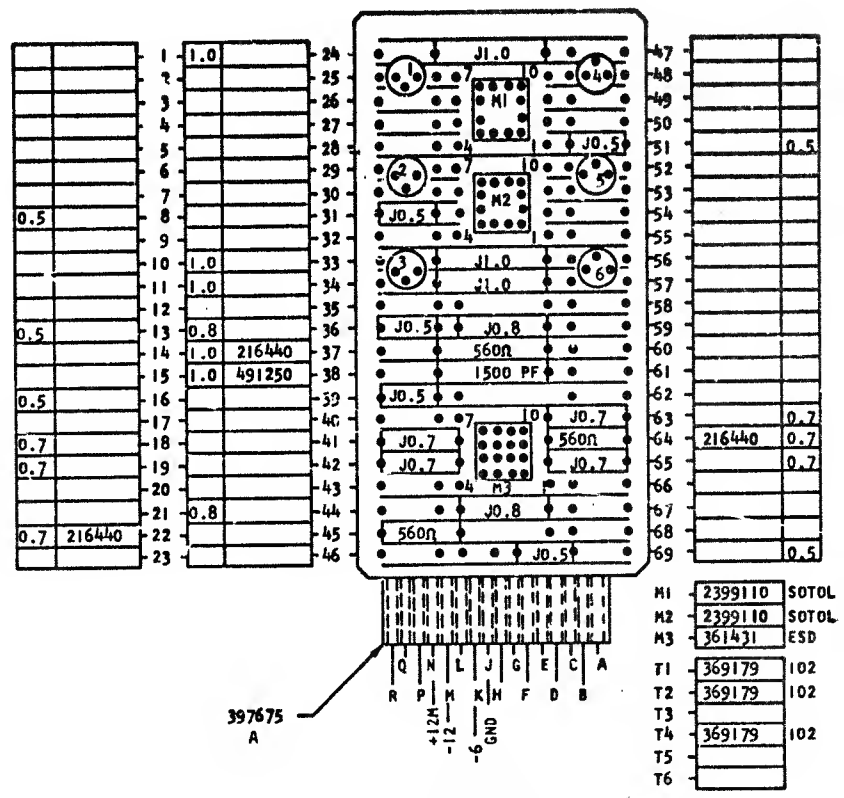
LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.



M1	2399110	SOTOL
M2	2399110	SOTOL
M3	361431	ESD
T1	369179	102
T2	369179	102
T3		
T4	369179	102
T5		
T6		

COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	2APR62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SOTDL-3-WAY LOGIC BLOCK LOW SPEED WITH LOADS					29JUN62	115599					729915
				MODEL	SMS	3JAN63	116034					
DESIGN				SCALE	NON.	21OCT63	118933					
DETAIL	RQ	1MAR62		DRAW	LIG 5MAR68	20FEB68	132162					
CHECK	WH	1MAR62		CHECK		12JUN68	132888	GWS				
APPRO	GS	10JUN68										

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2-0

STANDARDS CODE
2-6111

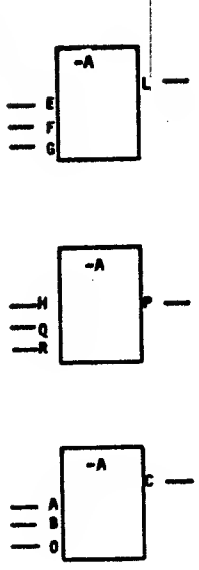
729916

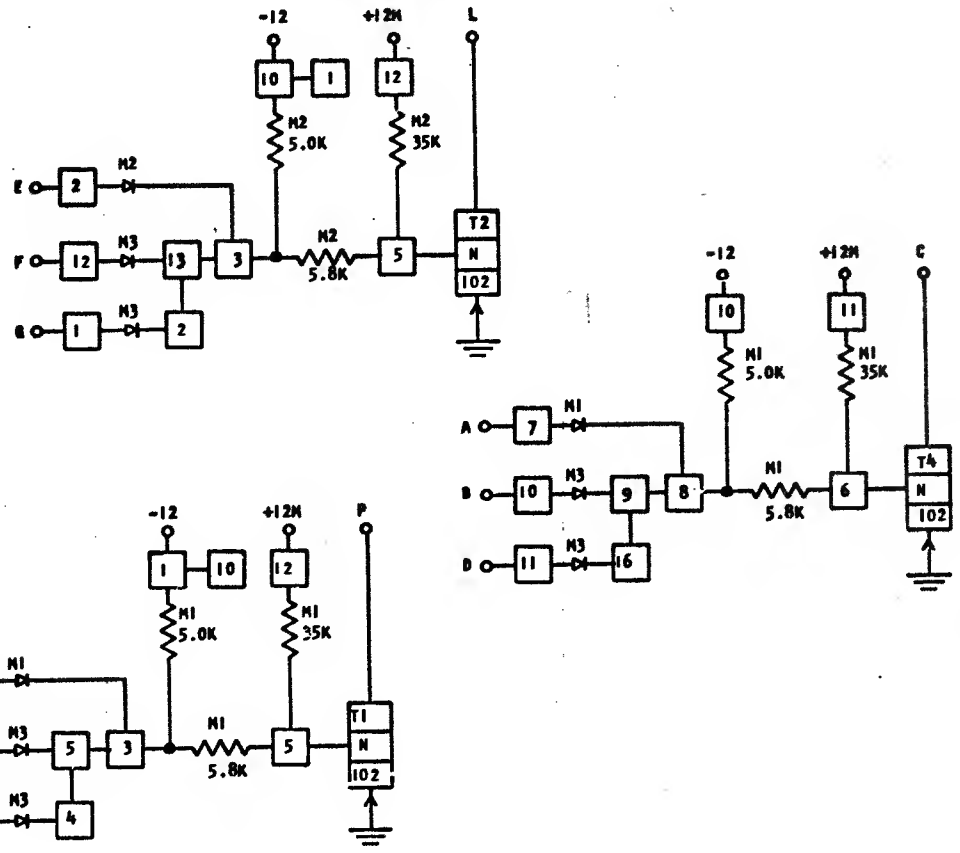
CARD CODE	729916
D G W -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370377

SDTDL 3-WAY LOGIC BLOCK LOW SPEED WITHOUT LOADS





SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
E,H, A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F,Q, B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,R, B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L,P, C	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

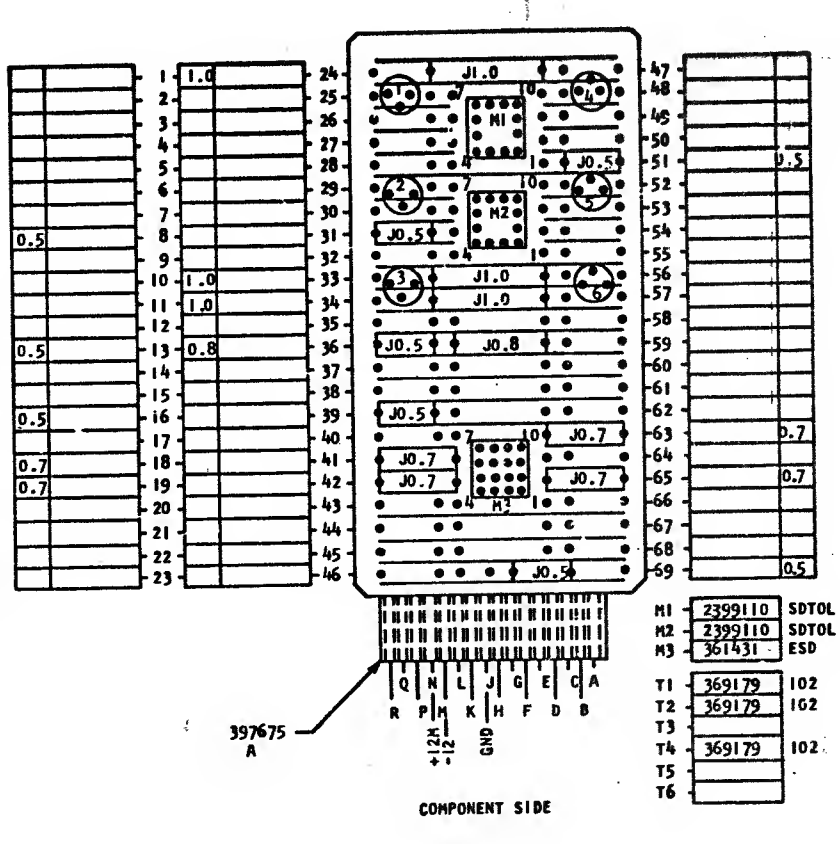
LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	2APR62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 3-WAY LOGIC BCK LOW SPEED WITHOUT LOADS					29JUN62	115599					
DESIGN			MODEL	SMS		3JAN63	116034					
DETAIL	RQ	1MAR62	SCALE	NONE		21OCT63	118933					
CHECK	WH	1MAR62	DRAW	LIG	5MAR68	3FEB68	132161					
APPRO	GS	10JUN62	CHECK			12JUN68	132888	GWS				

729916

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2-0

729917

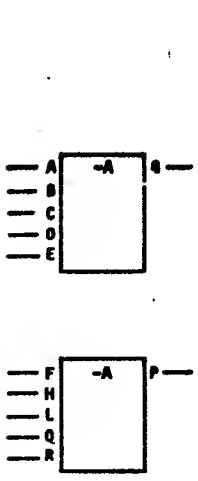
STANDARDS CODE 2-7045

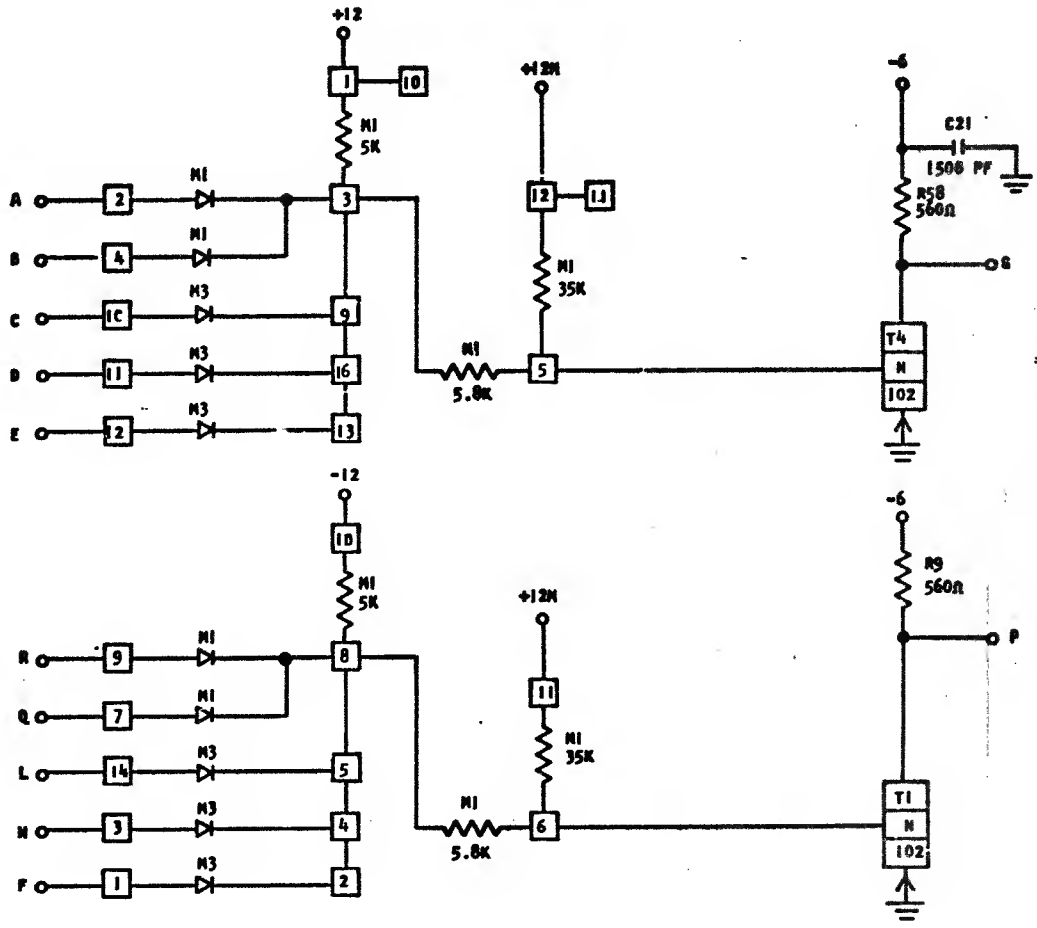
CARD CODE 729917

D G X -

REFERENCE DRAWING
SEE PRODUCTION DRAWING 370376

SDTDL-5-WAY LOGIC BLOCK LOW SPEED WITH LOADS

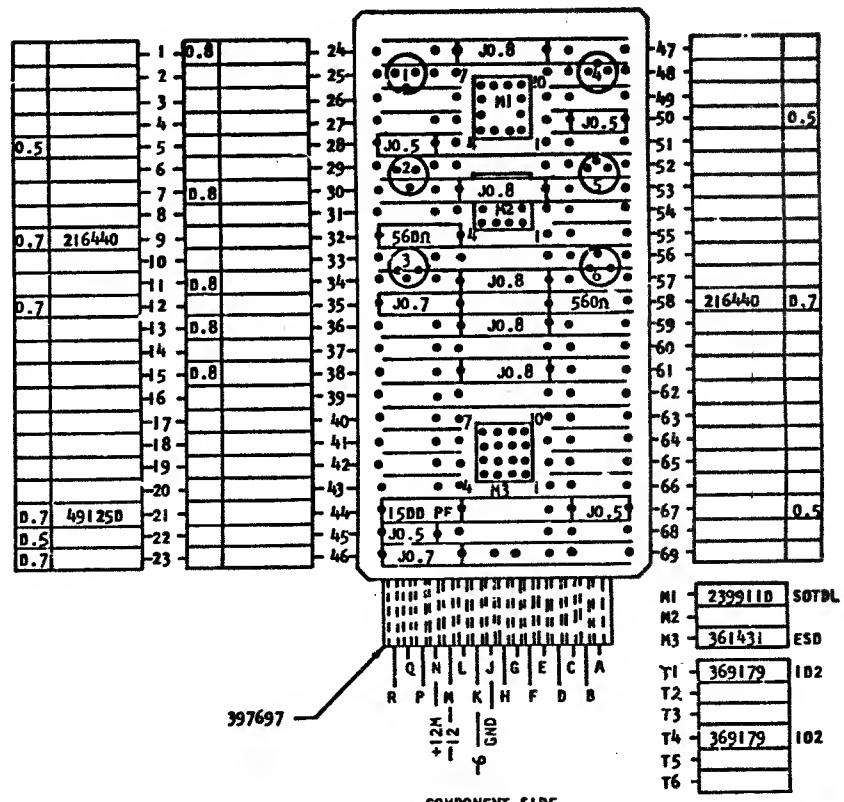




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C,L	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E,R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



COMPONENT SIDE

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	2APR62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 5-WAY LOGIC BLOCK LOW SPEED WITH LOADS				29JUN62	115599					
					30JUL63	117803					
DESIGN			MODEL	SMS	15SEP64	121632					
DETAIL	RQ	IMAR62	SCALE	NONE	1APR66	126401J	GLK				CIRCUIT FAMILY
CHECK	WH	IMAR62	DRAW	LIG 230CT67	12FEB68	132160					SDTDL
APPRO			CHECK	JD 260CT67							

729917

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OSILVIE PRESS, INC., BROOKLYN 17, N. Y. STOCK NO 4507

2-0

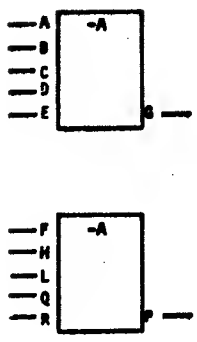
STANDARD CODE 2-7045

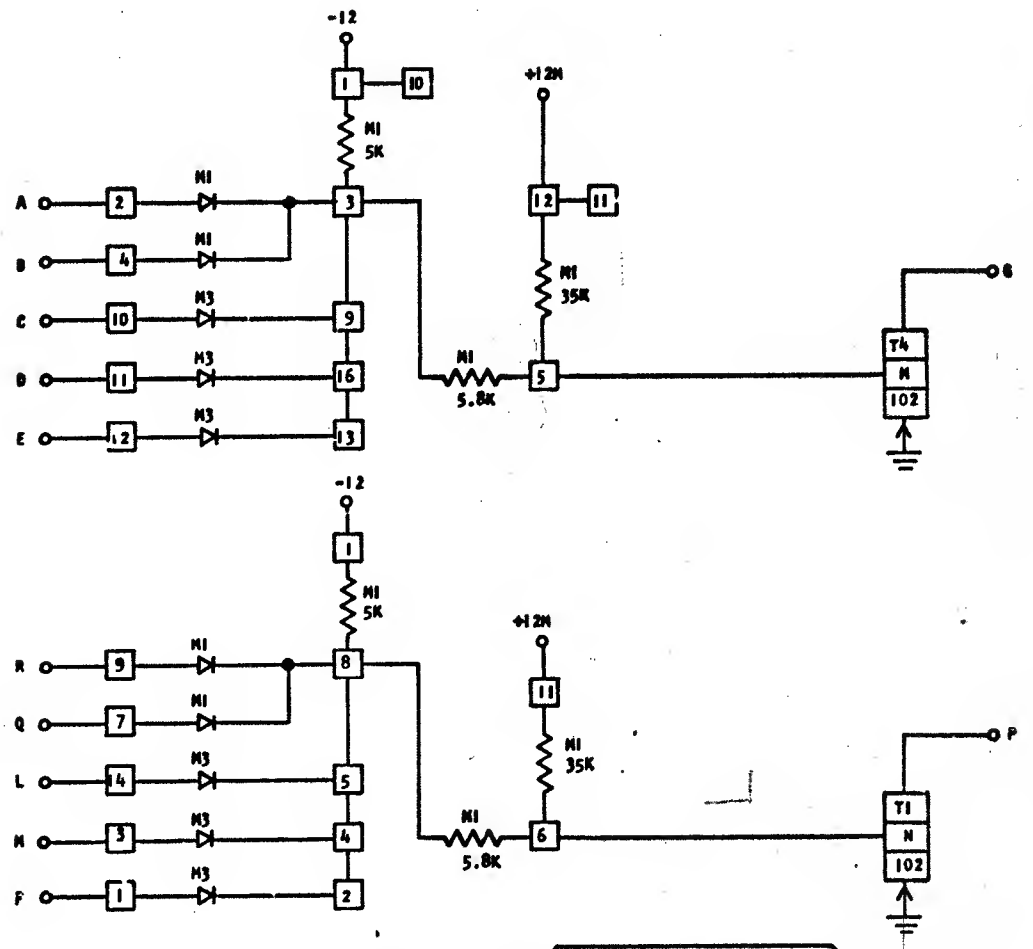
729918

CARD CODE D G Y - 729918

REFERENCE DRAWING
SEE PRODUCTION DRAWING 370375

SDTDL 5 WAY LOGIC BLOCK LOW SPEED WITHOUT LOAD

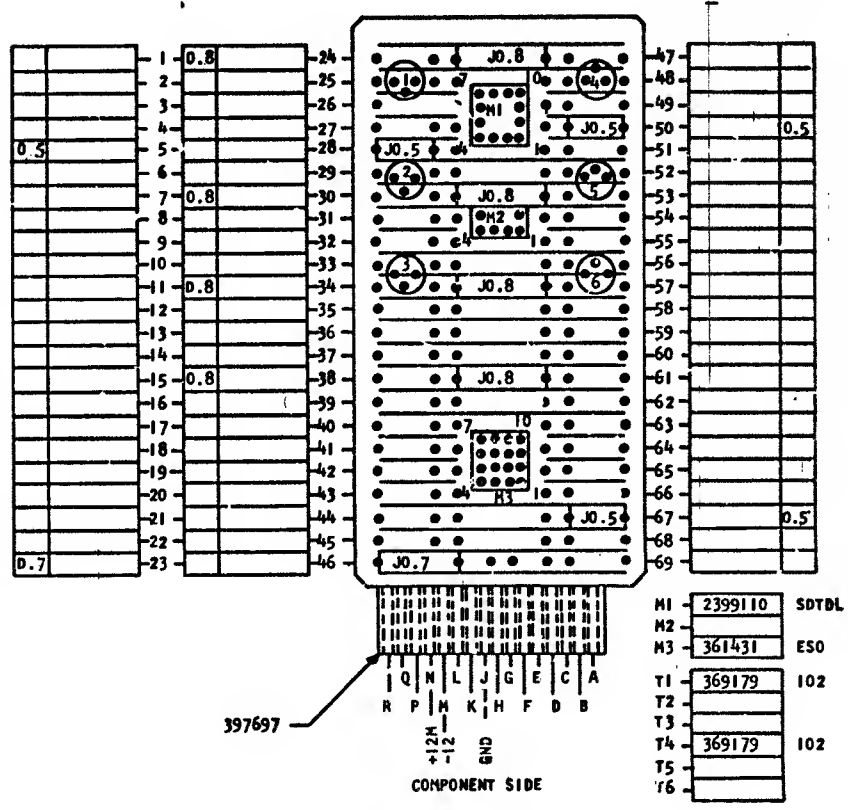




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
B,N	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
C,L	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
D,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
E,R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
G,P	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.8I	-8.8



DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.

C

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	2APR62

INTERNATIONAL BUSINESS MACHINES CORP.

NAME	CARD ASM TSTR-SDTDL 5-WAY LOGIC BLOCK LOW SPEED WO/LOAD				
DESIGN			MODEL	SMS	
DETAIL	RQ	1MAR62	SCALE	NONE	
CHECK	WH	1MAR62	DRAW	LIG	23OCT67
APPRO			CHECK	JD	26OCT67

DA	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
29JUN	115599					
30JUL	117803					
15SEP	121632					
1APR6	126401J	GLK				CIRCUIT FAMILY
	132159					SDTDL

729918

2-0

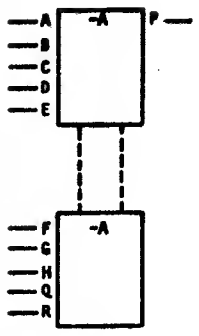
STANDARDS CODE	729919

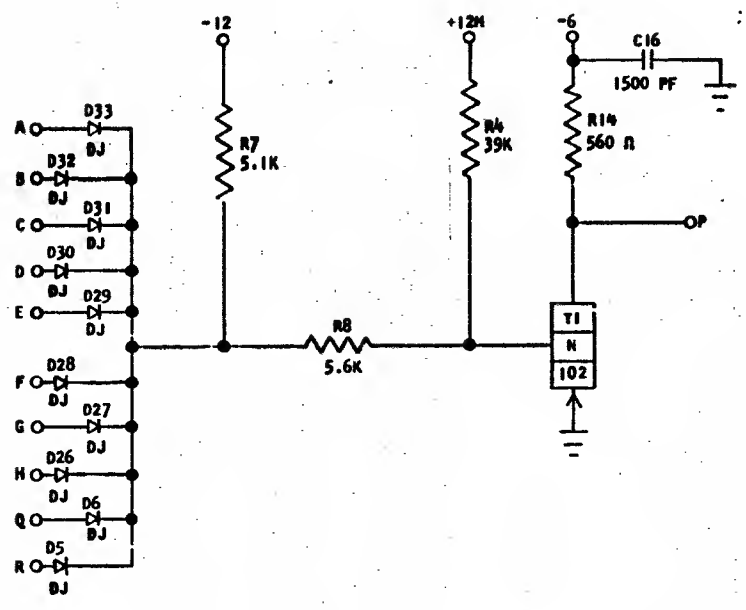
CARD CODE	729919
D G Z -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370373

10 WAY LOGIC BLOCK LOW SPEED WITH LOAD





DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

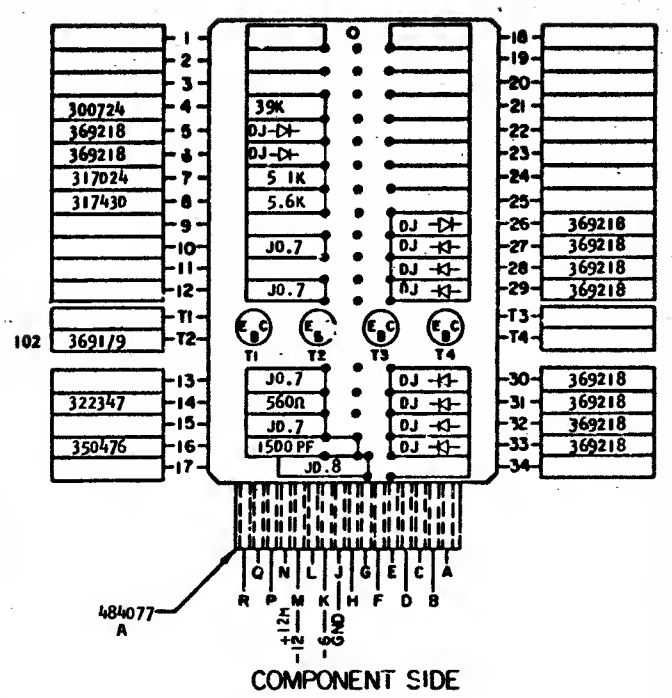
*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPJT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS HAV HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F	V	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
P	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729919
NAME	CARD ASM TSTR 10-WAY LOGIC BLOCK LOW SPEED WITH LOAD					6-29-62	115599						
DESIGN				MODEL	SMS	12-30-63	119217						
DETAIL	RQ	3-1-62		SCALE	NONE								
CHECK	WH	3-1-62		DRAW	LIG 3-17-62							CIRCUIT FAMILY	
APPRO				CHECK								SDTDL	

C

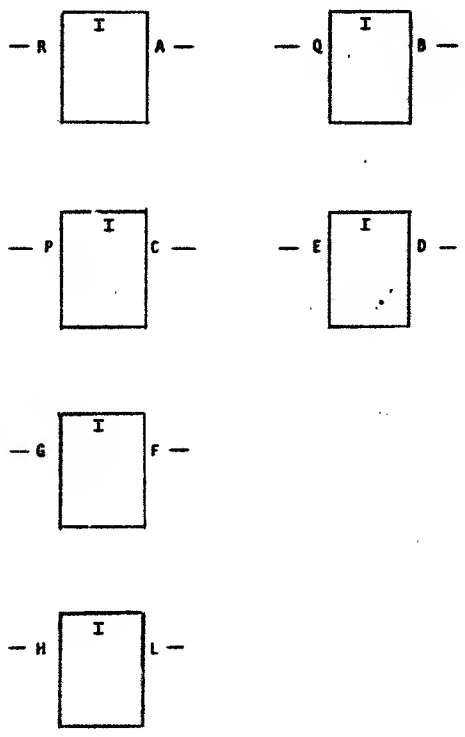
2-2

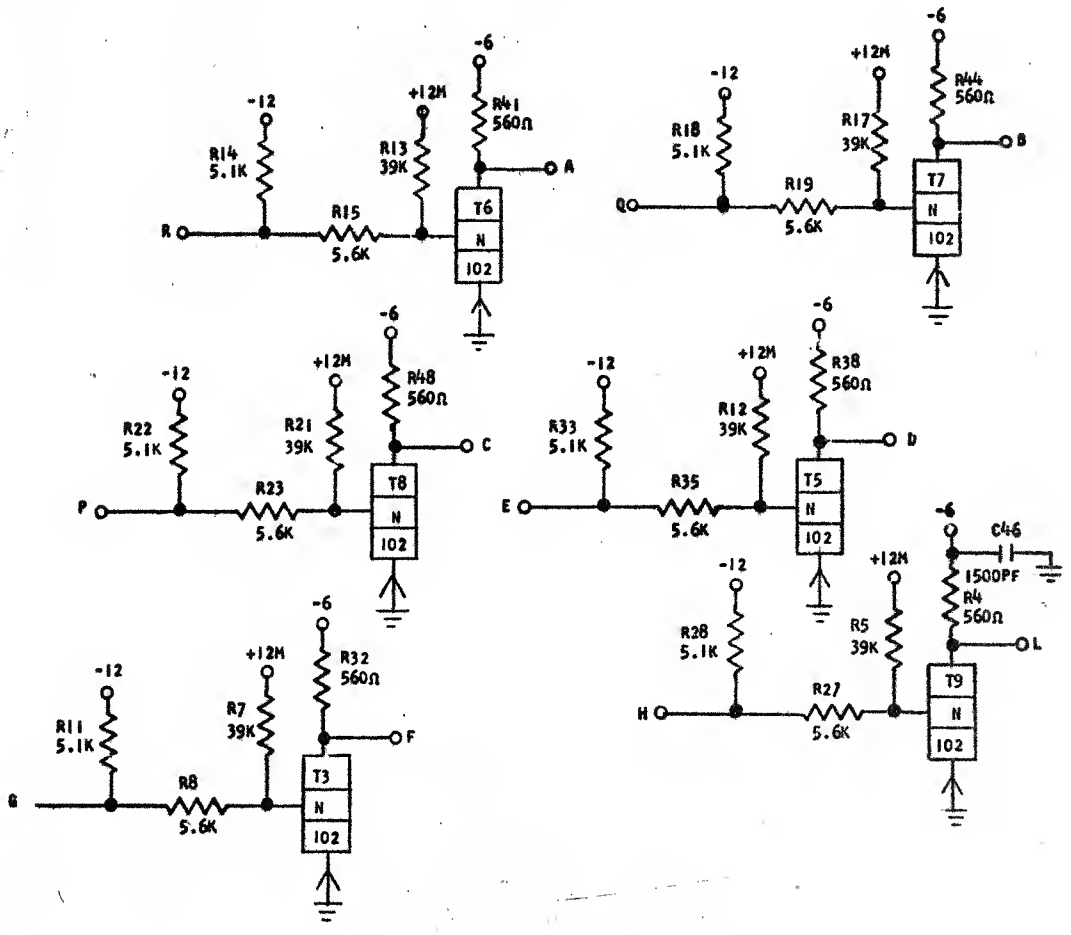
STANDARDS CODE
729921

CARD CODE	729921
D H B -	

INVERTER LOW SPEED WITH LOAD

REFERENCE DRAWING
SEE PRODUCTION DRAWING 370348





SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
R,Q,P, E,G,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
A,B,C, D,F,H	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

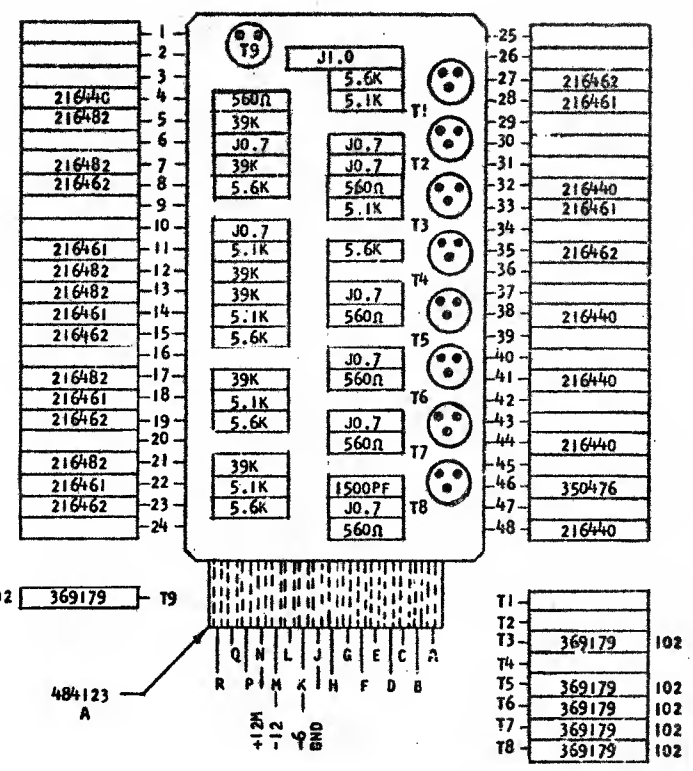
DELAY: SOTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100 *
TURN OFF (NSEC)	40	200 **

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR -					6-29-62	115599						729921
	INVERTER LOW SPEED WITH LOAD					1-3-63	116034						
DESIGN				MODEL	SMS								
DETAIL	RQ	3-1-62		SCALE	NONE	7-12-63	116192						
CHECK	WH	3-1-62		DRAW	JAB 3DEC65	8-31-64	121906					CIRCUIT FAMILY SOTDL	
APPRO				CHECK	HDG 3DEC65	3DEC65	126401						

C

2-0

729922

STANDARDS CODE

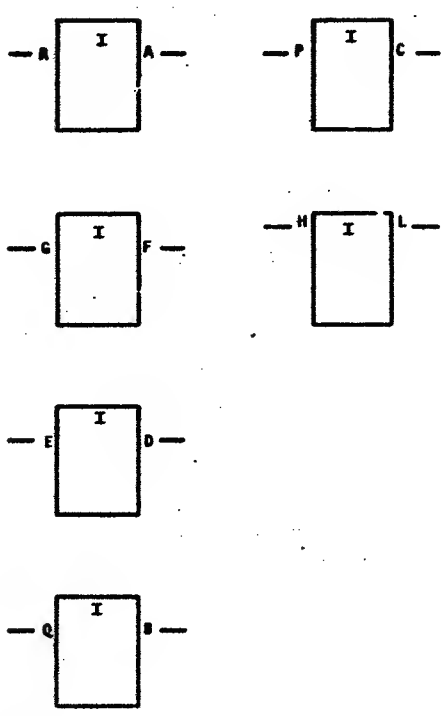
CARD CODE 729922

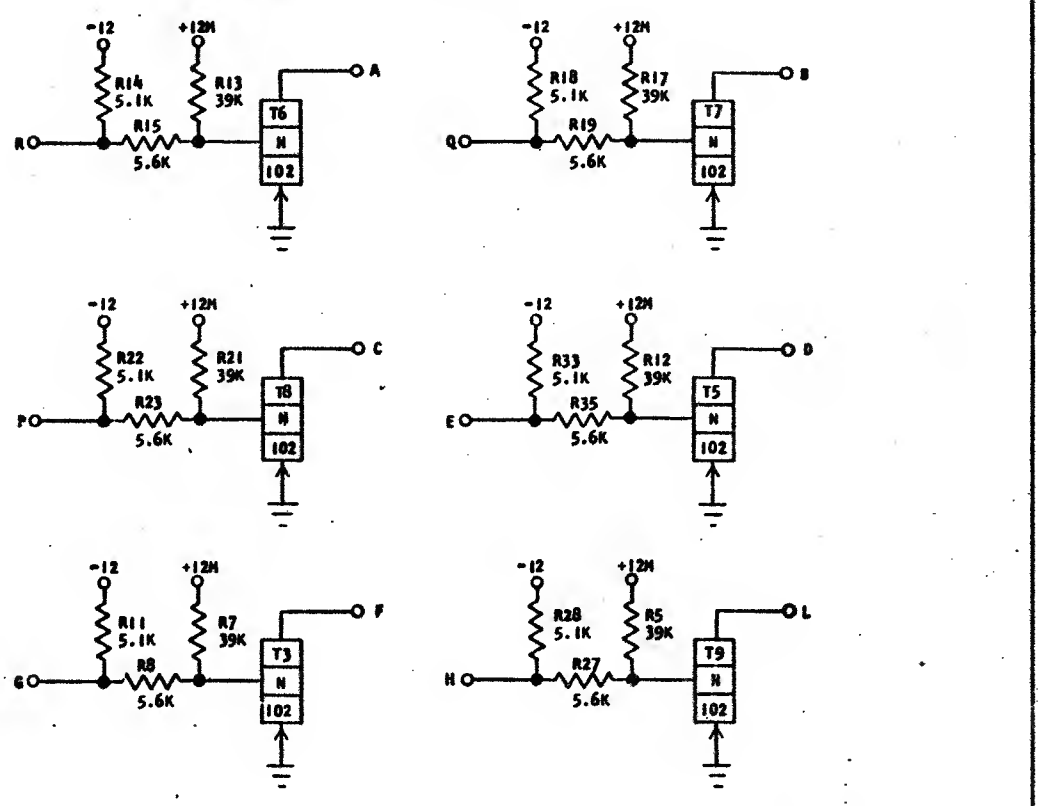
DHC -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370372

SDTDL INVERTER LOW SPEED W/O LOAD





SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. ALL COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
R,Q,P, E,G,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
A,B,C, D,F,L	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

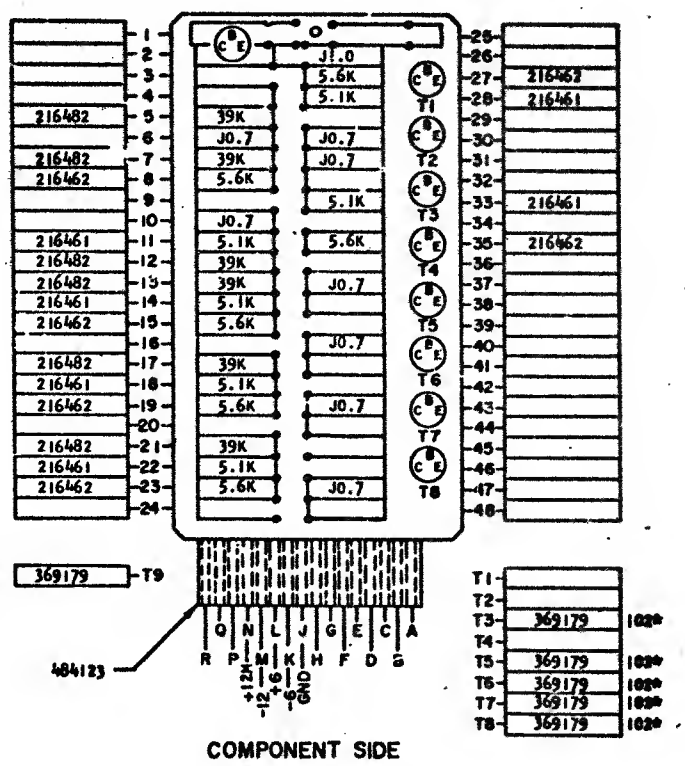
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR- SDTDL INVERTER LOW SPEED W/O LOAD					4-2-62	115599						729922
DESIGN			MODEL	SMS									
DETAIL	RQ	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIG	3-1-62								
APPRO			CHECK										

C

2-0

729925

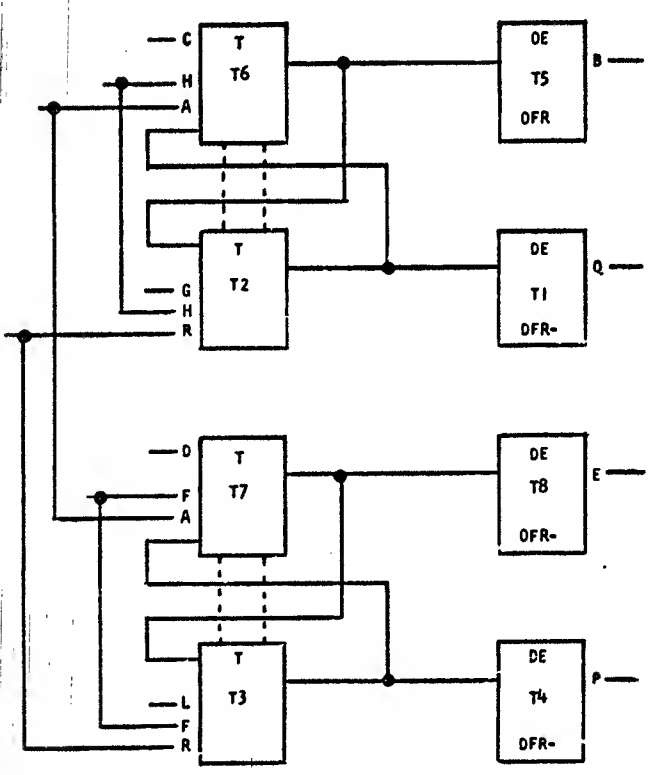
STANDARDS CODE
2-7045

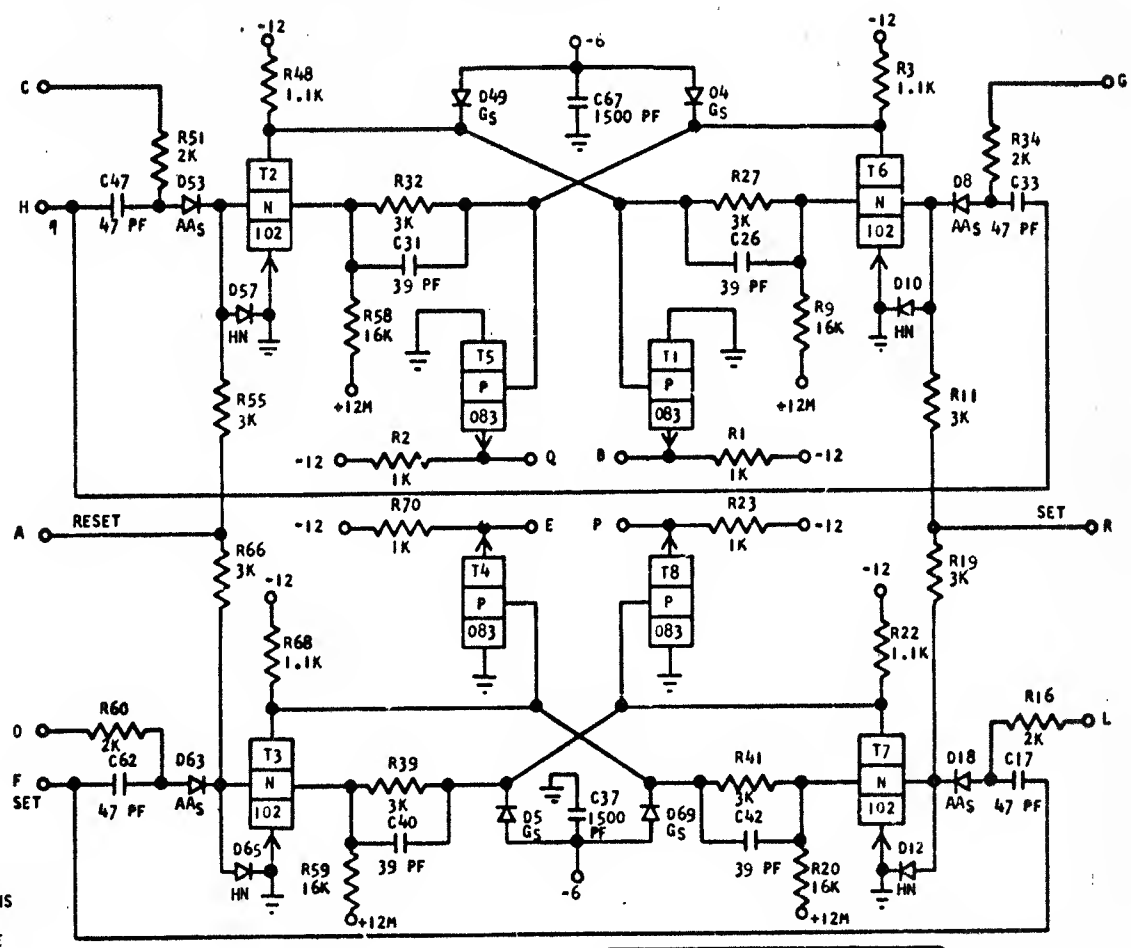
CARD CODE	729925
D H F -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370350

TRIGGER AND DRIVER





SEQUENCE OF OPERATION

THE RESET INPUT RESPONDS TO A NEGATIVE VOLTAGE LEVEL. RESETTING TURNS T6,T7,T5 AND T8 ON AND THE OTHER TRANSISTORS WILL BE IN THE OPPOSITE STATE. THE GATES ARE CONDITIONED BY A POSITIVE VOLTAGE LEVEL AND THE AC SET IS RESPONSIVE TO A POSITIVE VOLTAGE LEVEL. THUS, TO SET THE TRIGGER MEANS TO TURN OFF THE TRANSISTOR WHOSE GATE AND SET ARE BOTH POSITIVE. THE DC SET RESPONDS TO A NEGATIVE VOLTAGE LEVEL. THUS, WHEN THE TRIGGER IS DC SET, T2,T3,T1 AND T4 WILL BE ON.

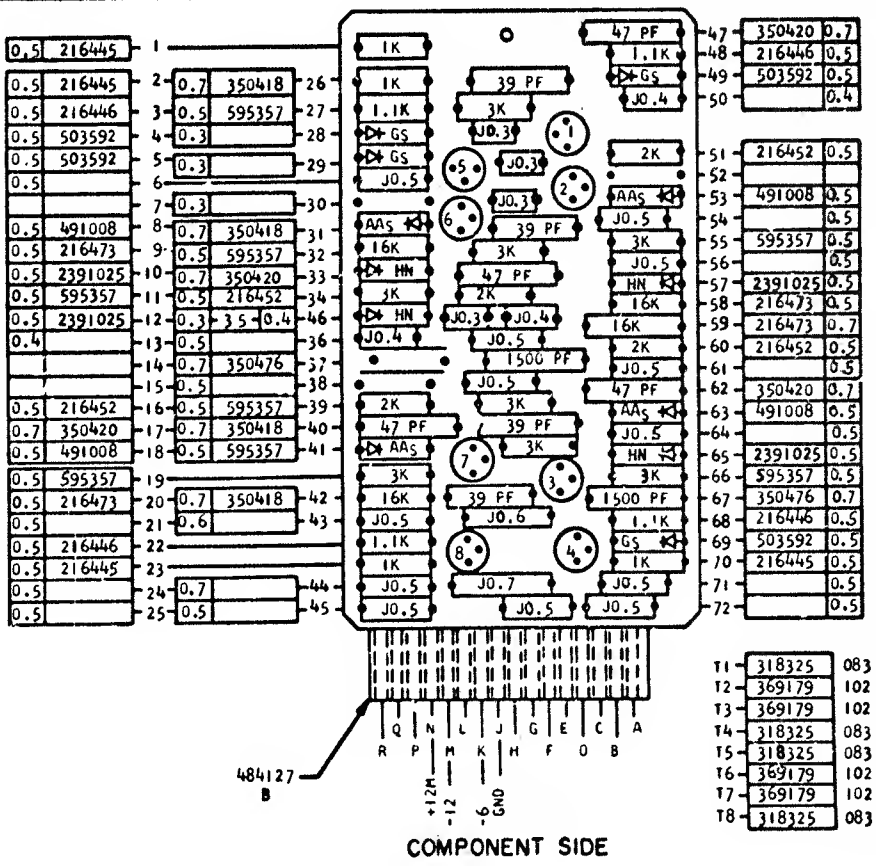
DELAY - NSEC	T_{DN} MAX	T_{DN} MIN	T_{RISE} MAX	T_{RISE} MIN	T_{OFF} MAX	T_{OFF} MIN	T_{FALL} MAX	T_{FALL} MIN
BINARY OPERATION:	123	36	63	16	240	115	200	95
GATED:	135	40	48	16	205	82	160	61

NOTE: T_{ON} IS DEFINED AS THE DELAY FROM THE TIME AN AC INPUT SIGNAL ARRIVES UNTIL THE "OFF" TRANSISTOR HAS TURNED ON COMPLETELY. THIS IS MEASURED FROM THE TIME THE AC INPUT HAS SHIFTED 10%.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
C,O	Y	GATE		UP	-.65	-.1
				DOWN	-5.81	-7.64
H,F	Y	AC SET		UP	-.65	-.1
				DOWN	-5.81	-7.64
R	Y	DC SET		UP	-.65	-.1
				DOWN	-5.81	-7.64
A	Y	RESET		UP	-.65	-.1
				DOWN	-5.81	-7.64
Q,P	Y	OUTPUT		UP	-1.1	-7.3
				DOWN	-5.83	-7.3
B,E	Y	OUTPUT		UP	-1.1	-.22
				DOWN	-5.83	-7.3
G,L	Y	GATE		UP	-.65	-.1
				DOWN	-5.81	-7.64

IN THE POSITIVE DIRECTION UNTIL THE "OFF" TRANSISTOR HAS SHIFTED 90% POSITIVE.

T_{OFF} IS MEASURED FROM THE TIME AN AC INPUT HAS SHIFTED 10% POSITIVE UNTIL THE OUTPUT OF THE "ON" TRANSISTOR HAS SHIFTED 90% NEGATIVE.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASSEMBLY TRANSISTOR - TRIGGER AND DRIVER					6-29-62	115599						729925
DESIGN			MODEL	SMS		1-3-63	116034						
DETAIL	RQ	3-1-62	SCALE	NONE		12.30.68	119217						
CHECK	WH	3-1-62	DRAW	LIG	2-17-62	9-15-64	121632					CIRCUIT FAMILY	
APPRO			CHECK			9AUG66	127574	GLK				SOTOL	

CARD CODE 729928

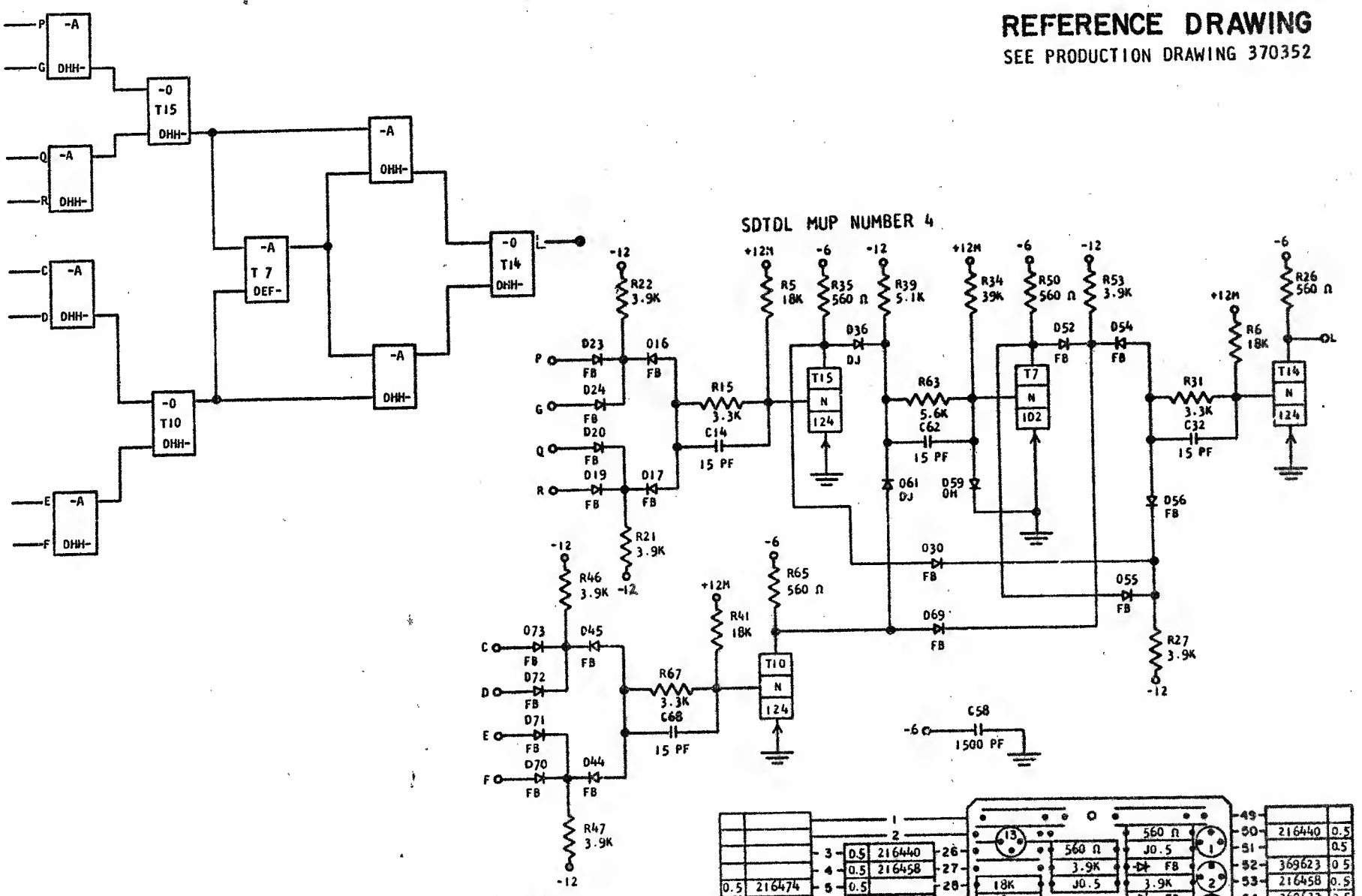
D H J -

STANDARDS CODE

729928

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370352



SEQUENCE OF OPERATION

1. THE FIRST LEVEL OF DIODES OF BOTH T15 AND T10 PERFORM A NEGATIVE AND, AND THE SECOND LEVEL OF DIODES PERFORM A NEGATIVE OR INVERT FUNCTION. THE DIODES OF T7 AND T7 PERFORM A NEGATIVE AND INVERT FUNCTION. THE OUTPUTS OF T15 AND T10 DRIVE THE DIODES OF T7. THE OUTPUTS OF T15, T10 DRIVE THE DIODES OF T7. THE OUTPUTS OF T15, T10 AND T7 ARE FED INTO THE FIRST LEVEL OF DIODES OF T14 WHICH PERFORMS A NEGATIVE AND FUNCTION. THE SECOND LEVEL OF DIODES AND T14 PERFORM A NEGATIVE OR INVERT FUNCTION. THIS CIRCUIT IS USED TO CHECK FOR ODD PARITY OF A TAPE CHARACTER. T15 AND T10 ARE EXCLUSIVE OR'S THAT EACH DETERMINE IF TWO BITS ARE ODD OR EVEN PARITY AND THEN T14, ANOTHER EXCLUSIVE OR, COMPARES THE OUTPUTS OF T15 AND T10 TO DETERMINE IF ALL FOUR BITS ARE EVEN OR ODD PARITY.
2. THE CARD CODES SHOWN IN THE BLOCKS REFER TO INDIVIDUAL CARDS SIMILAR TO THAT PORTION OF CIRCUITRY
3. DELAY - NSEC

INPUTS TO OUTPUT:	MIN.	MAX.
TURN ON	32	263
TURN OFF	27	213

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
P, G Q, R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C, O E, F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- SOTDL MUP NUMBER 3					SEE INDEX CARD					
					4-10-63	116155					
DESIGN			MODEL	SMS	11-5-63	118934					
DETAIL			SCALE	NONE	7-14-64	119024					
CHECK			DRAW	LIG 5-27-64							
APPRO			CHECK								

729928

C

2-0

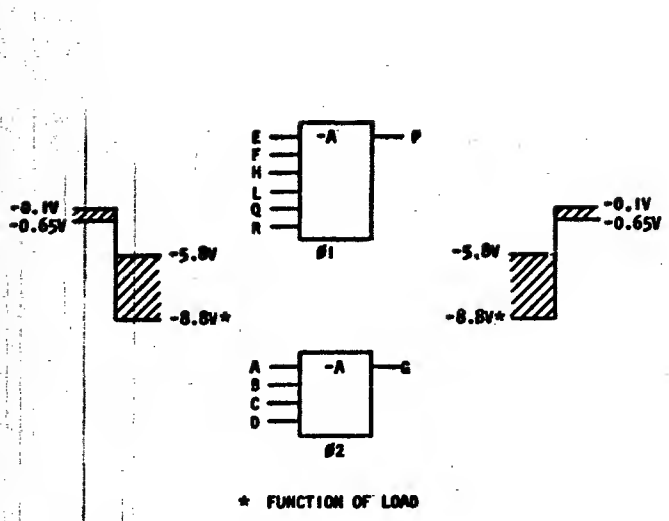
734301

734301

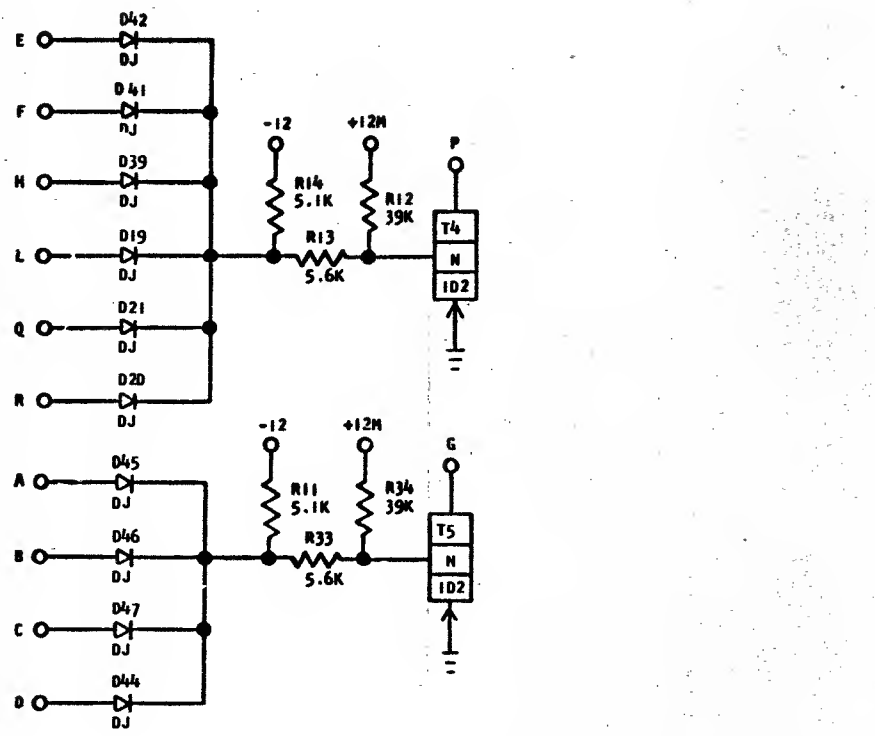
DHV-

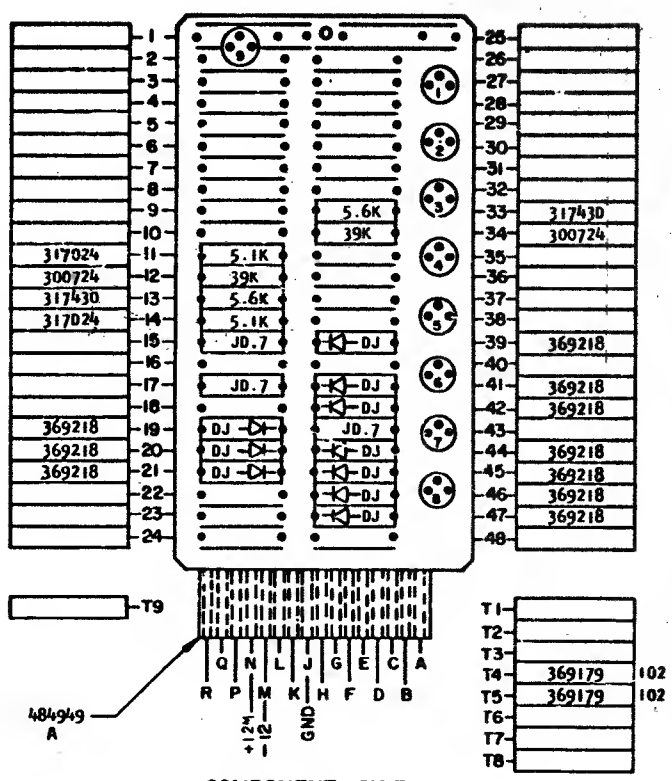
REFERENCE DRAWING
PRODUCTION DRAWING 372123

LS 1 6-WAY, 1 4-WAY NEGATIVE AND LOGIC BLOCKS WITHOUT LOADS



* FUNCTION OF LOAD





COMPONENT SIDE

OTHER DESIGNATIONS:

+0, -A0, +0A, +00, I, II, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	LS 1 6-WAY, 1 4-WAY NEG. AND LOGIC BLOCKS WITHOUT LOADS				3-25-63	116800						734301
					12-30-63	119217						
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE 12-10-62							CIRCUIT FAMILY	
APPRO	[illegible] 3-25-63		CHECK								SDTDL	

C

734354

734354

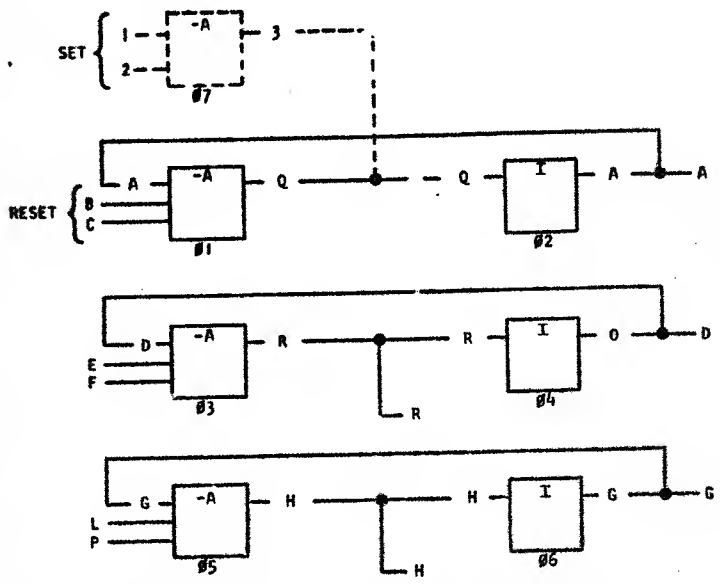
DHW—

P/N: 372191 EC: D114410A

REFERENCE DRAWING
PRODUCTION DRAWING 372191

SDTDL LATCH

TYPICAL APPLICATION*



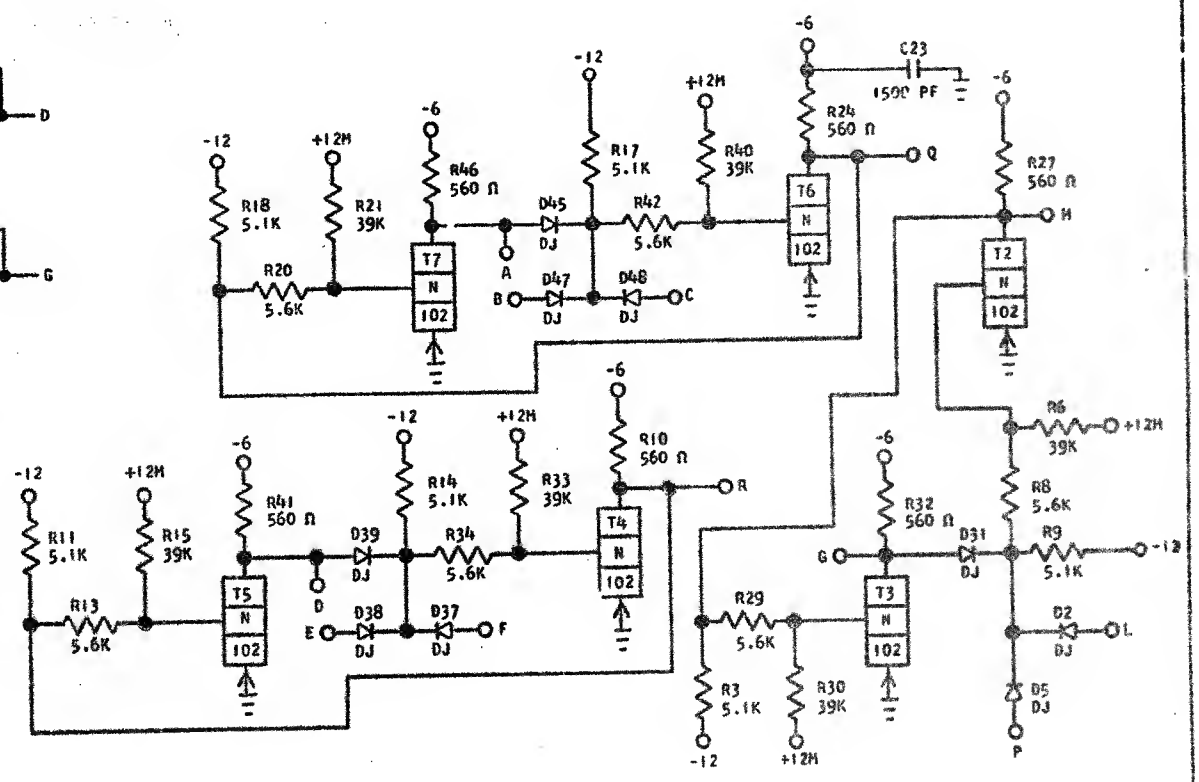
* CONFIGURATION Ø7 IS NOT A PART OF THE CARD AND IT MUST BE AN UNLOADED LOGIC BLOCK.

OTHER DESIGNATIONS

CONF. 1, 3, 5, 7	+0, -A0, +0A
CONF. 2, 4, 6	I, IO, IA

SEQUENCE OF OPERATION (TYPICAL APPLICATION)

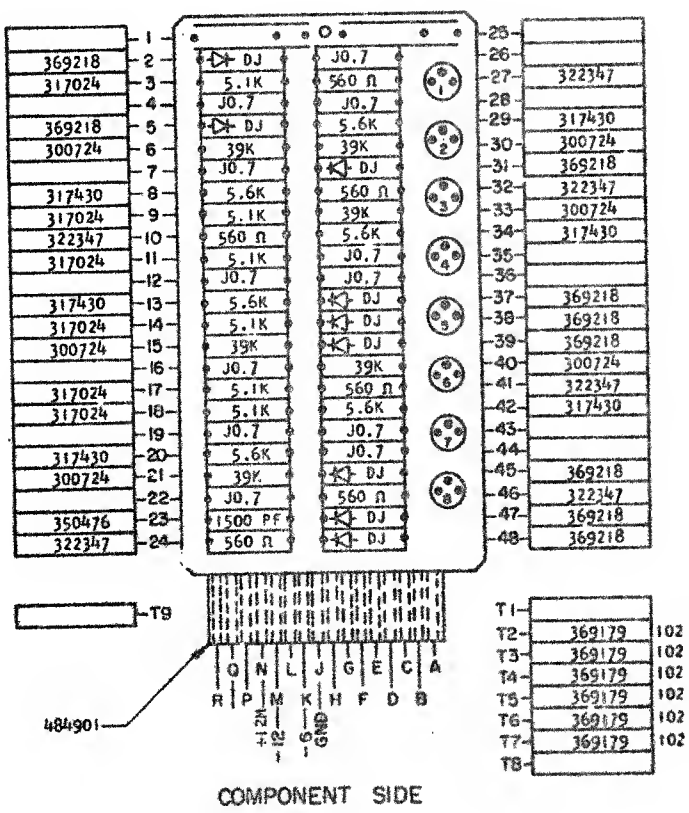
1. DOWN LEVEL ON PINS 1 AND 2 CAUSES TRANSISTOR IN SET BLOCK TO TURN ON, OUTPUT (TIED TO PIN Q OF LATCH) TO BE UP.
2. AN UP LEVEL AT INVERTER INPUT RESULTS IN DOWN LEVEL AT THE OUTPUT.
3. ALL INPUTS TO -A BLOCK OF LATCH DOWN, TRANSISTOR TURNS ON. LATCH IS NOW SET.
4. ALL LEVELS ON LATCH REMAIN STABLE, EVEN WHEN SET INPUT LEVELS CHANGE.
5. AN UP LEVEL ON PINS B OR C CAUSES TRANSISTOR IN -A BLOCK OF LATCH TO TURN OFF, OUTPUT (PIN Q) GOES DOWN. LATCH IS NOW RESET.



PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
1	Y	SET INPUT		UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V
2	Y	SET INPUT	SET SET	UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V
A	Y	OUTPUT	STORAGE	UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V
B	Y	RESET INPUT	RESET	UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V
C	Y	RESET INPUT	RESET	UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V
Q	Y	OUTPUT	STORAGE	UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V

DELAY - NSEC

		MIN	MAX
PINS A, B OR C TO PIN Q	TURN ON	75	100
	TURN OFF	40	200
PIN Q TO PIN A	TURN ON	75	100
	TURN OFF	40	200



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME SDTDL LATCH					11-17-63	116800A					734354
					5-2-63	116801					
DESIGN			MODEL	SMS 1440							
DETAIL			SCALE	NONE							
CHECK			DRAW	MDE 2-7-63							
APPRD	11-17-63		CHECK								

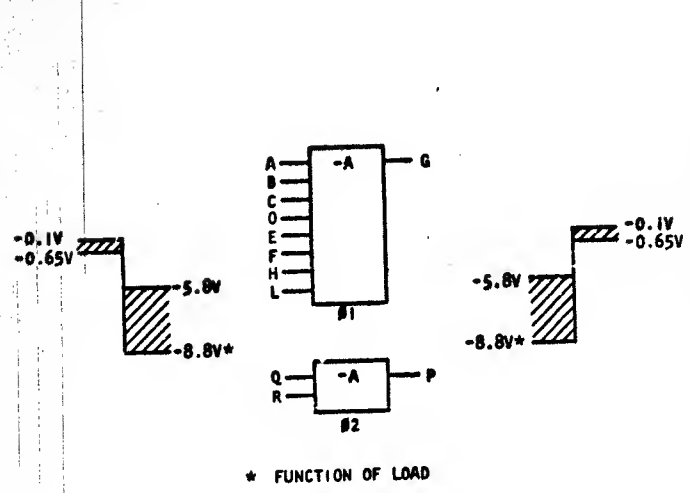
C

DHY-

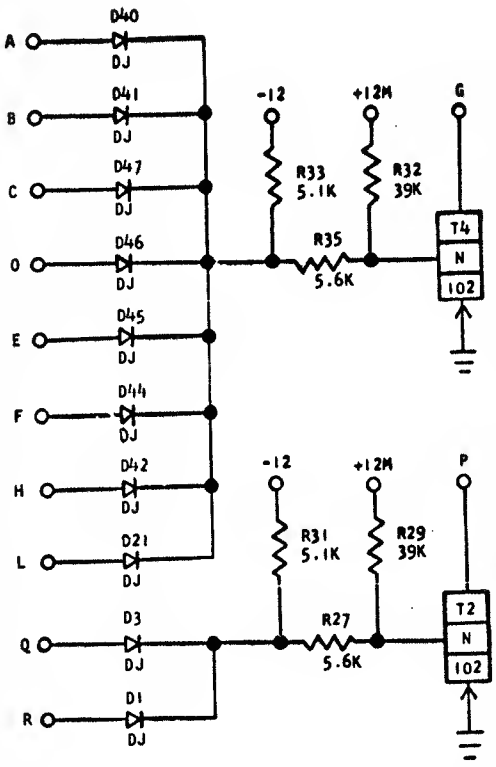
P/N:372193 EC:0114678

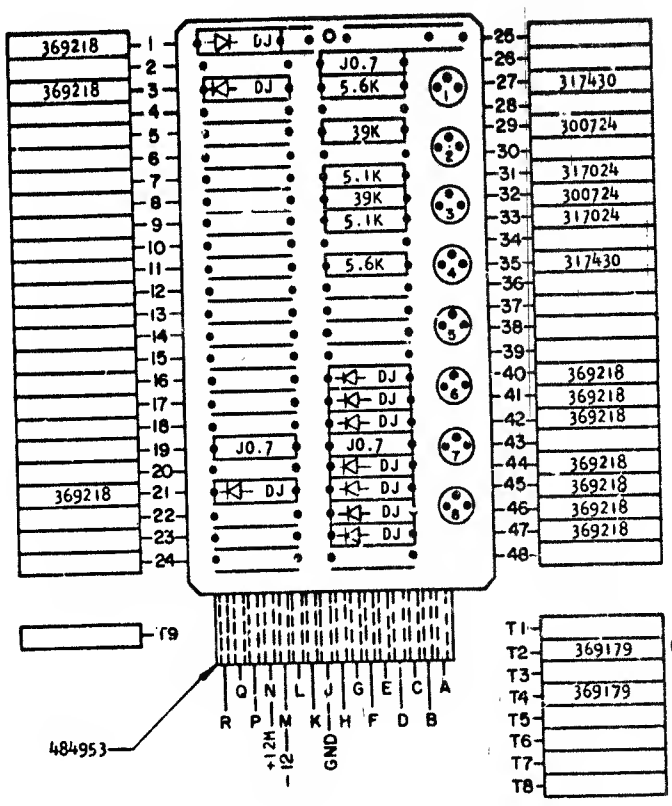
REFERENCE DRAWING
PRODUCTION DRAWING 372193

SDTDL LS I 8-WAY, I 2-WAY NEGATIVE AND LOGIC BLOCKS WITHOUT LOADS



* FUNCTION OF LOAD





COMPONENT SIDE

OTHER DESIGNATIONS:

+0, -A0, +0A, +00, I, ID, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

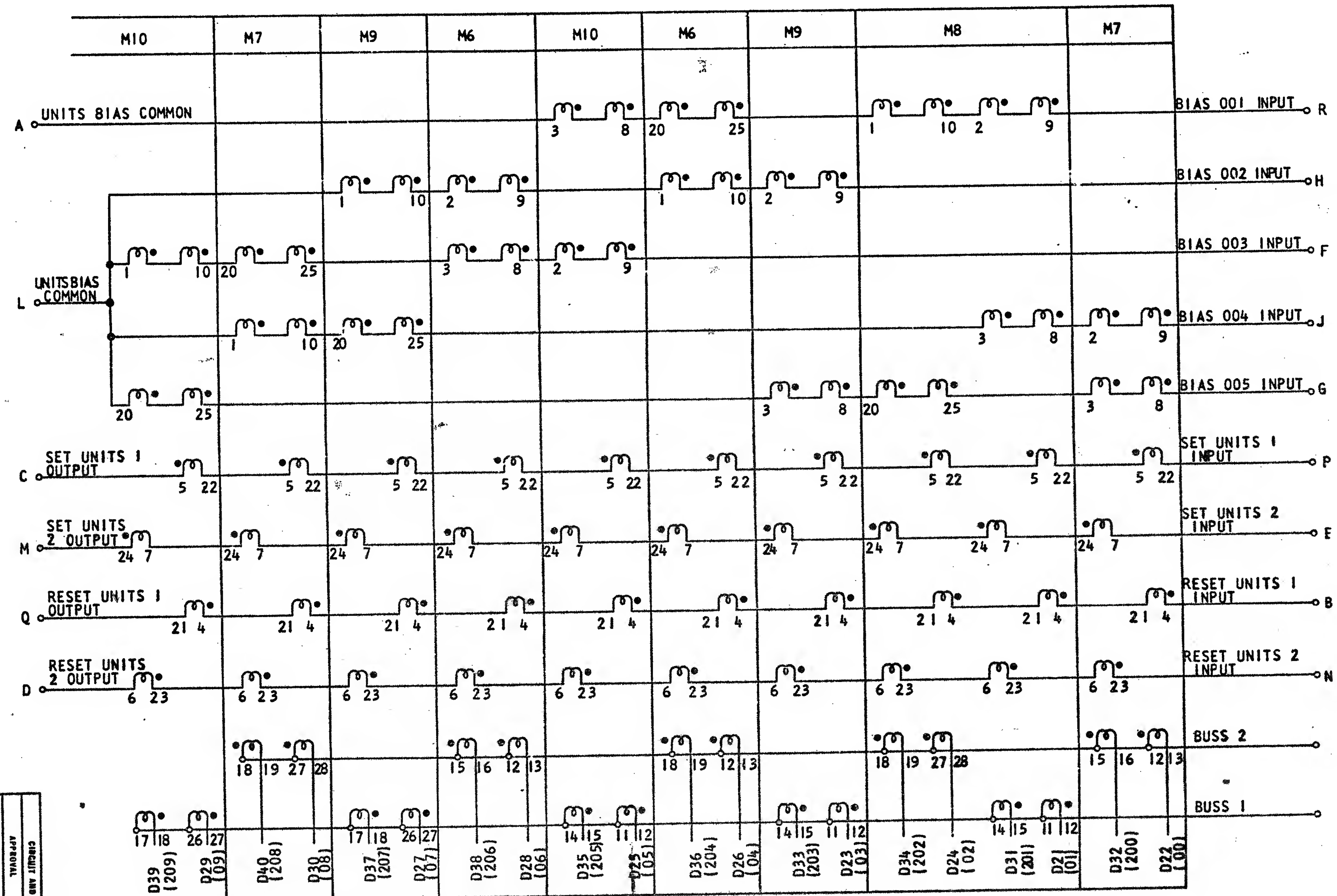
INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734302
NAME	SDTDL LS I 8-WAY, I 2-WAY NEG AND LOGIC BLOCKS WITHOUT LOADS				3-25-63	116800						
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			ORA'	MDE 12-10-62								
APPRO	[illegible] 3-25-63		CHECK									

C

SHEET 1 OF 3 373329

STANDARDS CODE 2-7045

SWITCH CORE MATRIX UNITS



NOTES

NUMBERS NEXT TO COIL INDICATE THE PINS ON THE MODULE INDICATED.

THIS IS NOT A POINT TO POINT WIRING DIAGRAM.

CARD CODE D J A- 373329

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
AC (GS)	4-17-62

INTERNATIONAL BUSINESS MACHINES CORP.			
NAME	TWIN CARD ASM- BUFFER MATRIX SWITCH CARD		
DESIGN	RK 12-11-61	MODEL	SMS
DETAIL	JWS 12-26-61	SCALE	NONE
CHECK		DRAW	LIG 1-24-64
APPRD	GWS 7-3-62	CHECK	

DATE	CHANGE NO.	APPROVAL
SEE	INDEX CARD	
10-28-63	D118973	GWS
2-21-64	D119688	BWS
31AUG65	125289	GLK
7FEB66	D125848	GLK

DATE	CHANGE NO.	APPROVAL
9FEB67	126567	GWS
13APR67	D131143	GWS

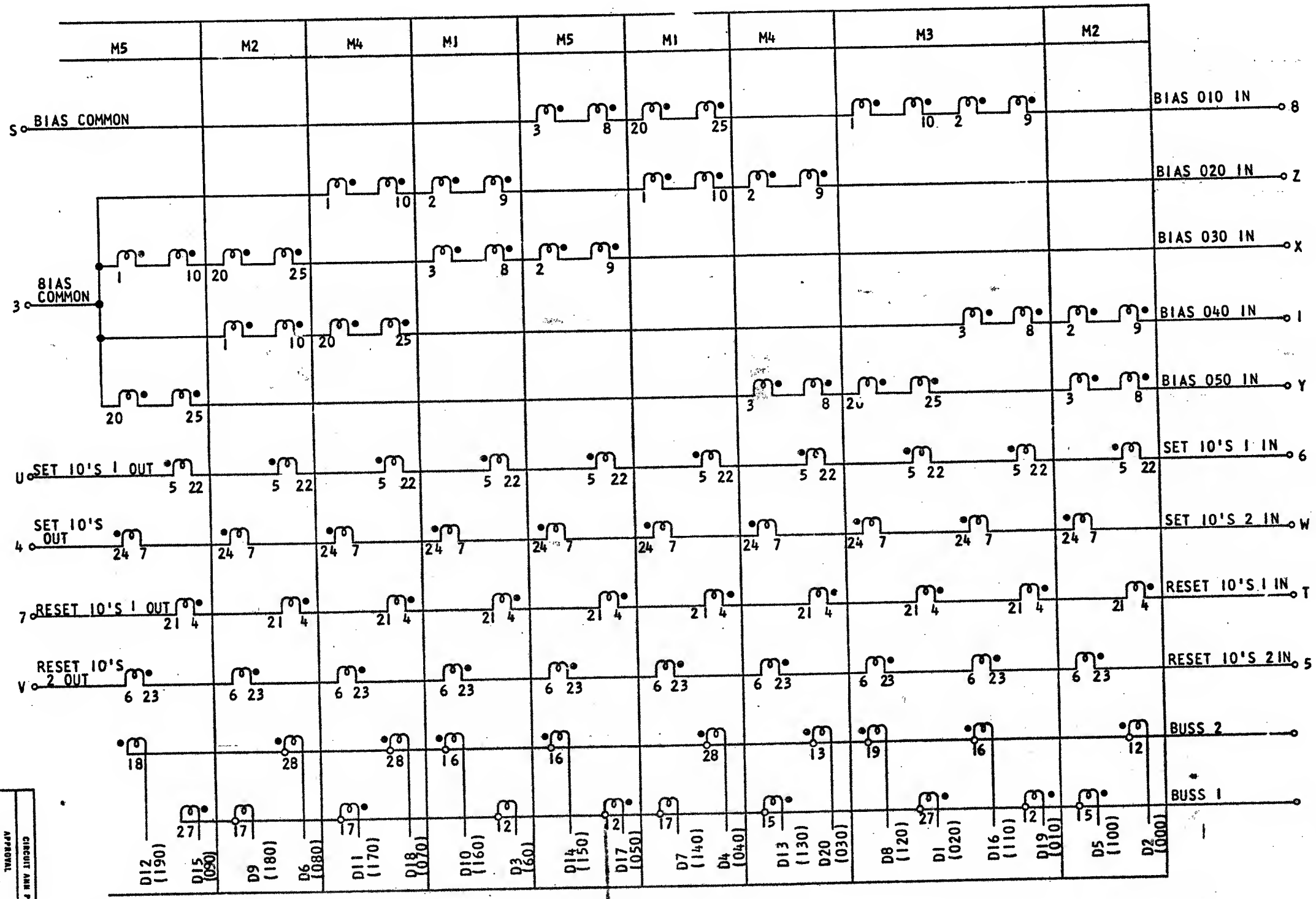
DEVELOPMENT NO. 13-450-0020

373329

C

STANDARDS CODE 2-7045

SWITCH CORE MATRIX TENS



NOTES

NUMBERS NEXT TO COIL INDICATE THE PINS ON THE MODULE INDICATED

THIS IS NOT A POINT TO POINT WIRING DIAGRAM

INTERNATIONAL BUSINESS MACHINES CORP.

NAME TWIN CARD ASM-BUFFER

MATRIX SWITCH CARD

DESIGN	R.K.	12-11-61	MODEL SMS
DETAIL	JWS	12-26-62	SCALE NONE
CHECK			
APP'D	GWS	1-3-62	DRAW L.IG 1-24-64
CHECK			

	APPROVAL	DATE	CHANGE NO.
	GLK	7FEB66	D125848
	GLK	31AUG65	125289
	GMS	10-28-63	D119688
	GMS	2-27-64	D119871
	GMS	13APR67	D131143
	GMS	9FEB67	125567

CIRCUIT ANN PACKAGING STANDARD		
APPROVAL	WAC (GS)	DATE 4-17-62

DEVELOPMENT NO. 13-450-0020

373329

FORM 80-001

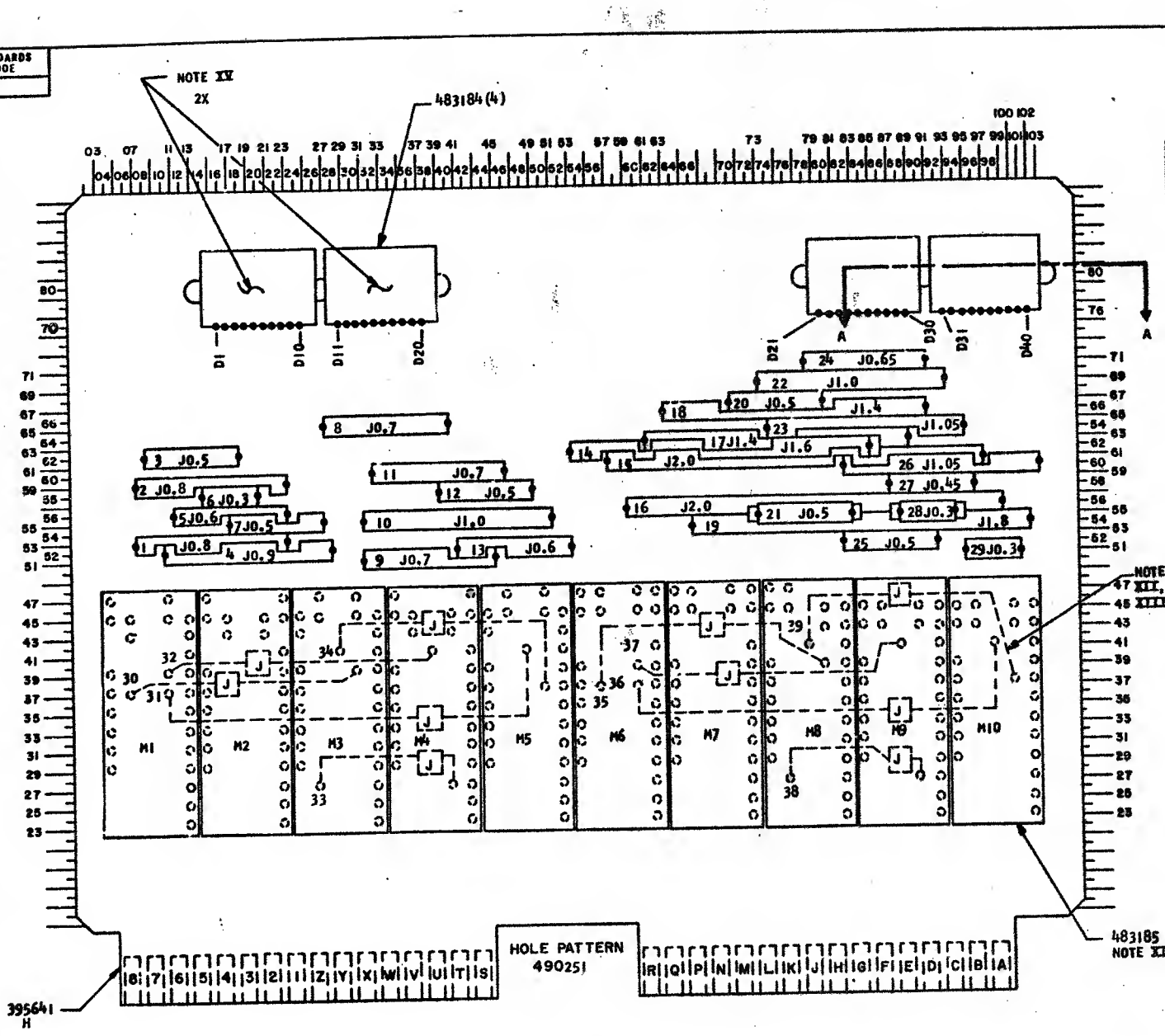
CARD CODE D J A- 373329

2.2

2-2

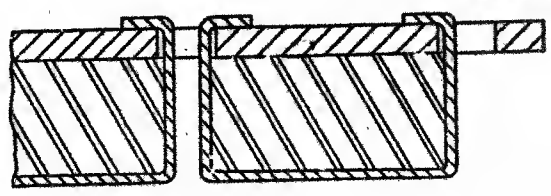
STANDARDS CODE	373329
CARD CODE	373329
D J A -	

SHEET 3 OF 3

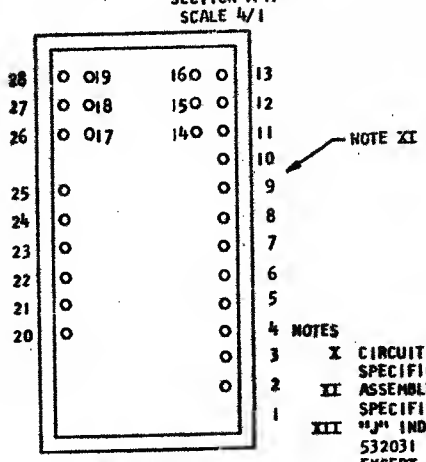


PART NO.	VALUE	QTY.

POSITION	VALUE	LEFT HOLE	RIGHT HOLE
1	J0.8	0753	2353
2	J0.8	0759	2359
3	J0.5	0862	1862
4	J0.9	1052	2852
5	J0.6	1156	2356
6	J0.3	1458	2058
7	J0.5	1755	2755
8	J0.7	2765	4165
9	J0.7	3151	4551
10	J1.0	3155	5155
11	J0.7	3260	4660
12	J0.5	3958	4958
13	J0.6	4152	5352
14	J1.6	5362	8562
15	J2.0	5761	9761
16	J2.0	5956	9956
17	J1.4	6163	8963
18	J1.4	6366	9166
19	J1.8	6654	10254
20	J0.5	7067	8067
21	J0.5	7355	8355
22	J1.0	7369	9369
23	J1.05	7464	9564
24	J0.65	7871	9171
25	J0.5	8252	9252
26	J1.05	8260	10360
27	J0.45	8758	9658
28	J0.3	8855	9455
29	J0.3	9551	10151
30	J	0637	3039
31	J	1037	4841
32	J	1039	3841
33	J	2627	4027
34	J	2841	5037
35	J	5637	8039
36	J	6037	9841
37	J	6039	8841
38	J	7627	9027
39	J	7841	10037



SECTION A-A
SCALE 4/1



TOP VIEW

XIV REFER TO FIELD SERVICE DRAWING 734415 WHEN MAKING CHANGES TO THIS ASSEMBLY.

XV APPLY FIBRE INSULATOR PART NUMBER 814286 TOPS OF PART NUMBER 483184. MAKE 814286 PROJECT. .010 - .030 ABOVE TOP EDGE OF 483184 (EDGE AWAY FROM CARD TABS.)

NOTES

X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 893151, 893153

XII ASSEMBLE TO ENGINEERING SPECIFICATION 893149 AND 893001

XIII "J" INDICATES JUMPERS, PART NUMBER 532031 FOR POSITION 1 THROUGH 39 EXCEPT FOR POSITIONS 3,6,8,10,11, 12,20,21,22,24,25,27,28, AND 29 WHICH WILL USE PART NUMBER 491296. CUT LENGTHS AS REQUIRED FOR POSITIONS 1 THROUGH 39.

XIII ASSEMBLE JUMPERS PART NUMBER 491296 AND 532031, BEFORE MODULE, PART NUMBER 483185. JUMPERS MUST NOT INTERFERE WITH MODULE LEADS IN POSITIONS 30 THROUGH 39.

PW 13APR67

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
WAC GS	4-17-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	TWIN CARD ASM- BUFFER MATRIX SWITCH CARD				
DESIGN	PPH	12-26-61	MODEL	SMS	
DETAIL	PPH	12-29-61	SCALE	NONE	
CHECK	KCB	6-15-62	DRAW	VE	3-19-64
APPRO	GWS	6-25-62	CHECK		

DATE	CHANGE NO.	APPROVAL
SEE EC HISTORY		
28OCT63	D118973	GWS
21FEB64	D119688	GWS
31AUG65	125289	GLK
7FEB66	0125848	GLK

DATE	CHANGE NO.	APPROVAL
9FEB67	126567	GWS
13APR67	D131143	GWS

DEVELOPMENT NO.	373329
13-450-0020	

C

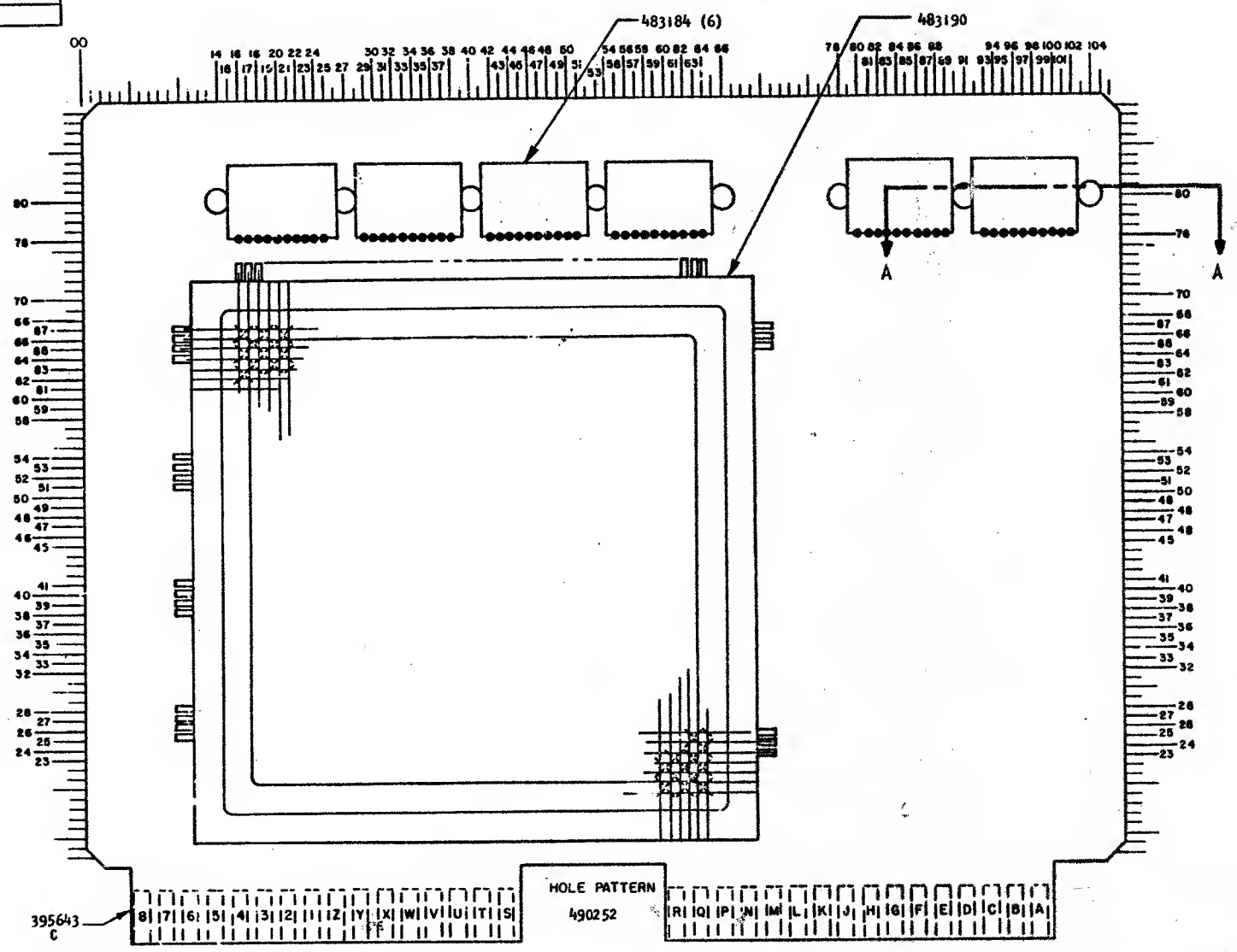
FORM 82-001

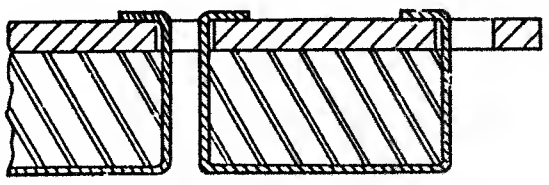
CARD CODE	373330
D J B -	

PART NO.	VALUE	QTY

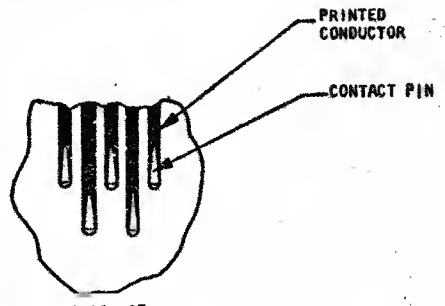
373330

STANDARDS CODE





SECTION A-A
SCALE 4/1



TYPICAL OF PRINTED SIDE NOTE XXI

NOTES
- X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATIONS 893157, 893153
- XI ASSEMBLE TO ENGINEERING SPECIFICATION 893001
- XXI CONTACT PIN AND PRINTED CONDUCTOR MUST BE ALIGNED WITHIN .015 PRIOR TO SOLDERING

MFG ENG	PW	12DEC68
CIRCUIT AND PACKAGING STANDARD		
APPROVAL		DATE
WAC GS		17APR62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	TWIN CARD ASM- BUFFER MEMORY CARD				
DESIGN	JWS	11-17-61	MODEL	SMS 1401G	
DETAIL	JWS	12-11-61	SCALE	NONE	
CHECK	RLV	12-21-61	DRAW	LIG	5-8-62
APPRO	JPM	12-22-61	CHECK		

DATE	CHANGE NO.	APPROVAL
9JUL62	114424	MDL
12-21-62	114424A	MDL
31AUG65	D125289	GLK
9JAN69	D133093	GWS

DATE	CHANGE NO.	APPROVAL

DEVELOPMENT NO.	373330
13-450-0013	

C

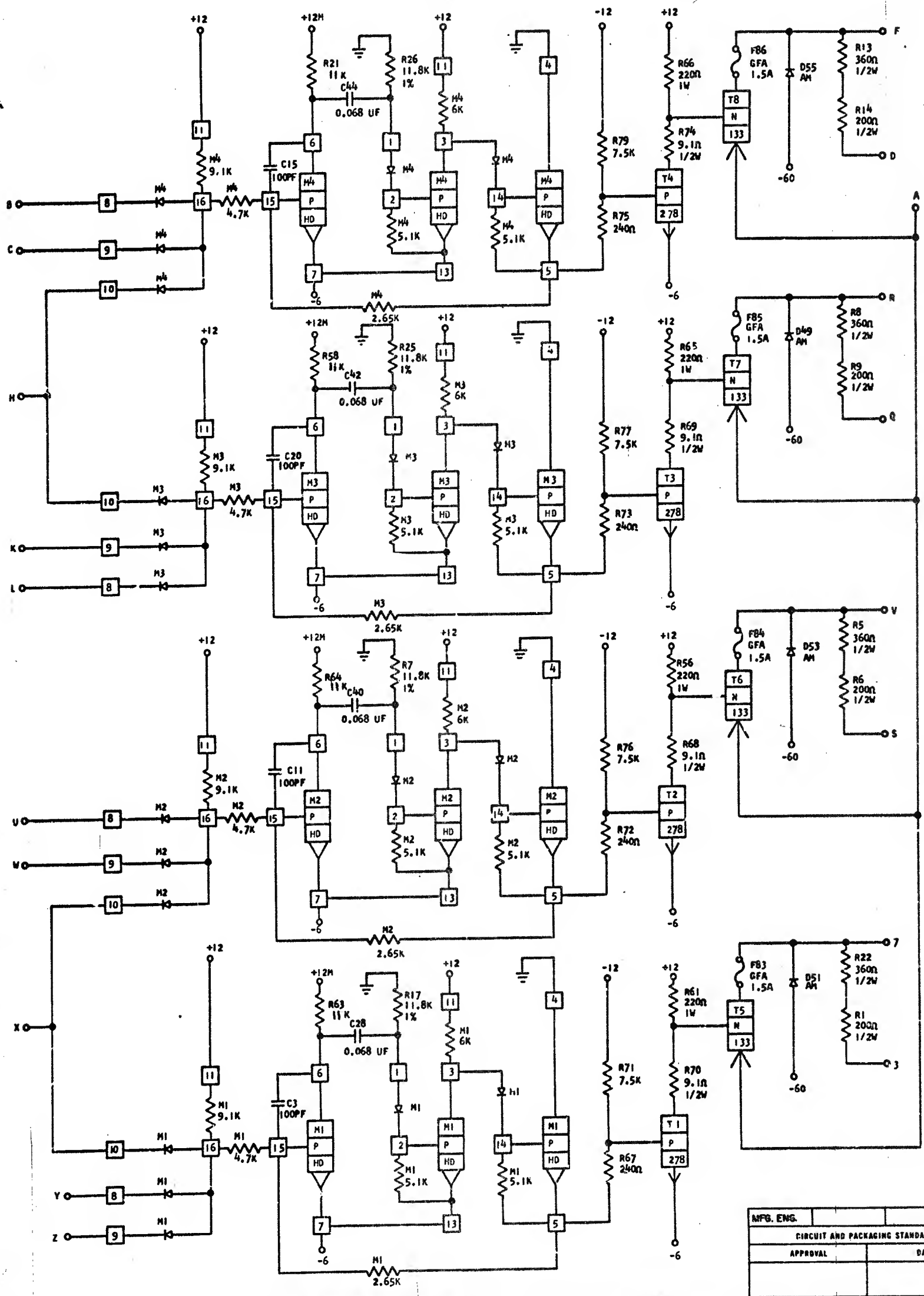
STANDARDS CODE 734404

SHEET 1 OF 3

SDTDL SINGLE SHOT HAMMER DRIVER

CARD CODE 734404

DJL-



VOLTAGE	PIN
GND	J 6 1
-6	2
+12	4
+12M	5
+12	6
-60	8

MFG. ENG.

CIRCUIT AND PACKAGING STANDARD

APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.

NAME SDTDL SINGLE SHOT HAMMER DRIVER

DESIGN | MODEL

DETAIL | SCALE

CHECK | DRAW

APPRO | CHECK

DATE	CHANGE NO.	APPROVAL
25APR63	1168008	
13MAR64	120097	CWS
21NOV64	122721	C K
26MAR65	123735	C K
	132174	

DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.

734404

STANDARDS CODE 734404

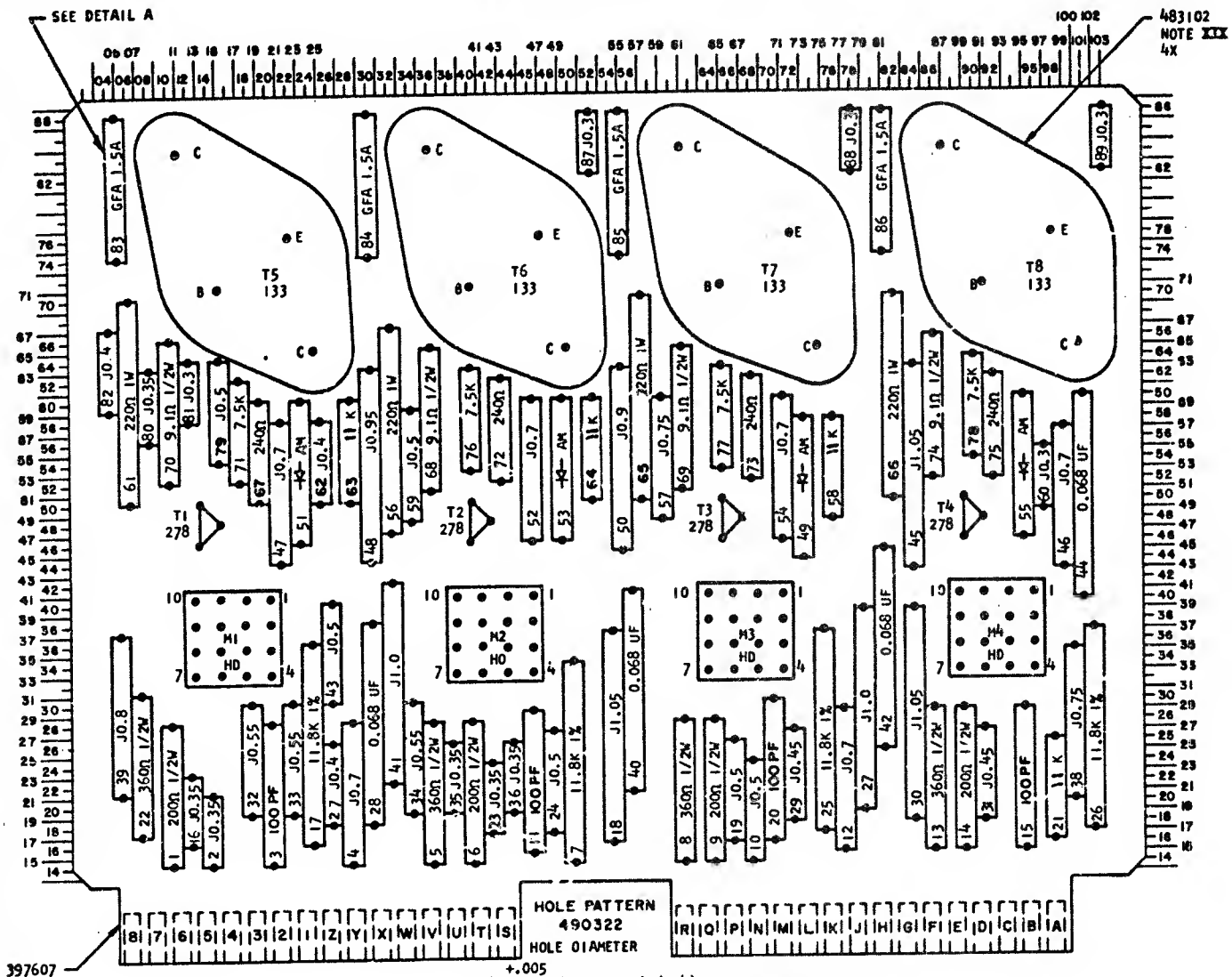
CARD CODE 734404

DJL-

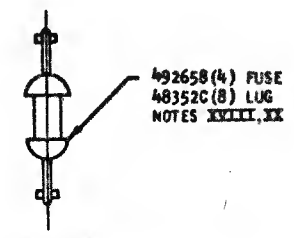
SHEET 2 OF 3

SDTDL SINGLE SHOT HAMMER DRIVER

RECOMMEND MOUNTING ON ONE INCH CENTERS (NOTE XVI)



PART NO.	VALUE	QTY.
216463	31K	4
216465	7.5K	4
317006	200Ω, 1/2W	4
321196	220Ω, 1W	4
482064	11.8K, 1%	4
483102	INSULATOR	4
483520	CONTACT	8
492504	0.068 UF	4
**492658	GFA 1.5	4
492693	9.1Ω, 1/2W	4
528937	360Ω, 1/2W	4
550050	240Ω	4
2111232	AM	4
5301506	100PF	4
2391057	278	4
2399113	HD	4
2414803	133	4



DETAIL A 4X

POSITION	VALUE	LOWER HOLE	UPPER HOLE
1	200Ω 1/2W	1014	1028
2	J0.35	1414	1421
3	100PF	2014	2028
4	J0.7	2814	2828
5	360Ω 1/2W	3614	3628
6	200Ω 1/2W	4014	4028
7	11.8K 1%	5014	5034
8	360Ω 1/2W	6114	6128
9	200Ω 1/2W	6414	6428
10	J0.5	6814	6824
11	100PF	4615	4629
12	J0.7	7715	7729
13	360Ω 1/2W	8615	8629
14	200Ω 1/2W	8915	6929
15	100PF	9515	9529
16	J0.35	1216	1223
17	11.8K 1%	2416	2436
18	J1.05	5416	5437
19	J0.5	6616	6626
20	100PF	7016	7030
21	11K	9816	9826
22	360Ω 1/2W	0717	0731
23	J0.35	4217	4224
24	J0.5	4817	4827
25	11.8K 1%	7517	7537
26	11.8K 1%	10217	10237
27	J0.4	2618	2626
28	0.068 UF	3018	3038
29	J0.45	7218	7227
30	J1.05	8418	8439
31	J0.45	9118	9127
32	J0.55	1819	1830
33	J0.55	2219	2230
34	J0.55	3419	3430
35	J0.35	3819	3826
36	J0.35	4419	4426
37	J1.0	7919	7939
38	J0.75	10020	10035
39	J0.8	0521	0537
40	0.068 UF	5621	5641
41	J1.0	3222	3242
42	0.068 UF	8125	8145
43	J0.5	2630	2640
44	0.068 UF	10140	10160
45	J1.05	8443	8464
46	J0.7	9943	9957
47	J0.75	2144	2159
48	J0.95	3044	3063
49	AM	7344	7358
50	J0.9	5545	5563
51	AM	2346	2360
52	J0.7	4646	4660
53	AM	4946	4960
54	J0.7	7146	7160
55	AM	9546	9560
56	220Ω 1W	3247#	3267#
57	J0.6	5948	5960
58	11K	7648	7658
59	J0.5	3449	3459
60	J0.3	9749	9755
61	220Ω 1W	0650#	0670#
62	J0.4	2550	2558
63	11K	2850	2860
64	11K	5250	5260
65	220Ω 1W	5750#	5770#
66	220Ω 1W	8250#	8270#
67	240Ω	1951	1961
68	9.1Ω 1/2W	3651	3665
69	9.1Ω 1/2W	6151	6165
70	9.1Ω 1/2W	1052	1066
71	7.5K	1752	1762
72	240Ω	4352	4362
73	240Ω	6852	6862
74	9.1Ω 1/2W	8652	8666
75	240Ω	9252	9262
76	7.5K	4053	4063
77	7.5K	6553	6563
78	7.5K	9053	9063
79	J0.45	1554	1563
80	J0.35	0856	0863
81	J0.3	1258	1264
82	J0.4	0459	0467
83	GFA 1.5A	0574#	0588#
84	GFA 1.5A	3074#	3088#
85	GFA 1.5A	5574#	5588#
86	GFA 1.5A	8174#	8188#
87	J0.3	5282	5288
88	J0.3	7882	7888
89	J0.3	10382	10388

POSITION	TYPE	E	B	C	C
T1	278	1346	1548	1350	
T2	278	4046	4248	4050	
T3	278	6546	6748	6550	
T4	278	8946	9148	8950	
T5	133	2276#	1571#	1184X#	X2465#
T6	133	4776#	4071#	3684X#	X4965#
T7	133	7276#	6571#	6184X#	X7465#
T8	133	9876#	9171#	8784X#	X10065#

MODULE POSITION	TYPE	CO-ORDINATES			
M1	HD	$2040X	$2038	$2035X	$2033
		SX1733	S1533	SX1233	SX1235X
		SX1238	SX1240X	S1540X	SX1740X
		SX1738	SX1735X	S1535X	S1538
M2	HD	S4640X	S4638	S4635X	S4633
		SX4333	S4133	SX3833	SX3835X
		SX3838	SX3840X	S4140X	SX4340X
		SX4338	SX4335X	S4135X	S4138
M3	HD	S7140X	S7138	S7135X	S7133
		SX6833	S6633	SX6333	SX6335X
		SX6338	SX6340X	S6640X	SX6840X
		SX6838	SX6835X	S6635X	S6638
M4	HD	S9640X	S9638	S9635X	S9633
		SX9333	S9133	SX8833	SX8835X
		SX8838	SX8840X	S9140X	SX9340X
		SX9338	SX9335X	S9135X	S9138

**XX MOUNT LEADS OF FUSE 492658 .170 (4,32) FROM SURFACE OF CARD

XXI FIELD REFERENCE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS

NOTES

X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 893168

XI ASSEMBLE TO ENGINEERING SPECIFICATION 89300;

XII ALL RESISTORS ARE 1/4 WATT ±5% UNLESS OTHERWISE NOTED

XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296

XIV DO NOT CRIMP EMITTER AND BASE TRANSISTOR LEADS 2414803, IN POSITION 15,T6,T7 AND T8

XV MODULES WILL BE MOUNTED WITH THE NUMBER 1 PIN IN THE UPPER RIGHT HAND CORNER.

XVI MAXIMUM HEIGHT COMPONENT MAY PROJECT ABOVE SURFACE OF CARD IS .375 (9,52)

XVIII REFER TO FIELD SERVICE DRAWING, PART NUMBER 734404 WHEN MAKING A CHANGE TO THIS CKT.

**XVIII MOUNT LUGS (8) PART NUMBER 483520 IN POSITIONS 83,84,85,86 WITH SLOT ALIGNMENT PARALLEL TO X-X AXIS BEFORE SOLDERING 1.5 AMP FUSES (4). PART NUMBER 492658 ARE TO BE SOLDERED TO LUGS. CENTER FUSE ALONG CENTERLINE OF FUSE LUGS

XIX CENTER DISC PART NUMBER 483102 ON TOP OF TRANSISTOR 2414803 INSURE THAT THE EDGES OF THE DISC ARE IN INTIMATE CONTACT WITH THE TRANSISTOR

MFG ENG	PW	
CIRCUIT AND PACKAGING STANDARD		
APPROVAL		DATE
SIZ		

C "X" INDICATES .025 (0,64) OFF GRID

INTERNATIONAL BUSINESS MACHINES CORP.			
NAME	SDTDL SINGLE SHOT HAMMER DRIVER		
DESIGN		MODEL	
DETAIL		SCALE	
CHECK		DRAW	
APPRO		CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
25APR63	116800B					734404
13MAR64	120097	GWS				
21NOV64	122721	GLK				
26MAR65	123735	GLK				
	132174					

734404

REFERENCE DRAWING
PRODUCTION DRAWING 373354

734404

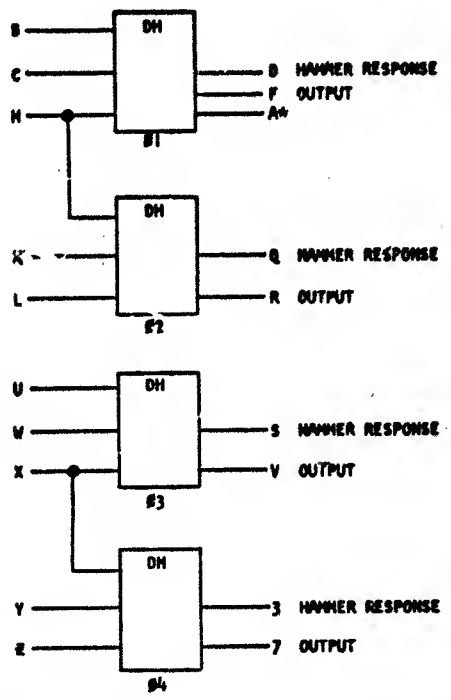
DJL—

P/N: 373354

SHEET 3 OF 3

SHEET 3 OF 3

SDTDL SINGLE SHOT HAMMER DRIVER



4. PIN A IS A SEPARATE LOW-IMPEDANCE GROUND PATH FOR THE OUTPUT TRANSISTORS. IT MUST BE GROUNDED BY CARD SOCKET WIRING.

SEQUENCE OF OPERATION

1. PINS B,C, OR H DOWN: CIRCUIT CANNOT BE PULSED.
2. PINS B, C, AND H UP: T4 TURNS ON AND CHARGES C46.
3. T8 THEN TURNS ON AND PROVIDES FEEDBACK TO KEEP T4 ON.
4. T12 ALSO TURNS ON WHICH IN TURN DRIVES T16.
5. CIRCUIT RESETS WHEN C46 DISCHARGES.

PINS	SIGNAL NAME		WAVESHAPE	LEVELS	MIN	MAX
B	Y	INPUT		UP	-.65V	-.1V
				DOWN	-5.81V	-12.48V
C	Y	INPUT		UP	-.65V	-.1V
				DOWN	-5.81V	-12.48V
H	Y	INPUT		UP	-.65V	-.1V
				DOWN	-5.81V	-12.48V
F		OUTPUT	1.16-1.6 MSEC	UP	-2V	0V
				DOWN	-.54V	-66V

NOTES
1. THE INPUT PULSE WIDTH MUST BE 1.5 USEC OR GREATER TO OPERATE CIRCUIT.
2. CIRCUIT CANNOT BE TRIGGERED MORE FREQUENTLY THAN EVERY 43 MSEC.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	SDTDL SINGLE SHOT HAMMER DRIVER				
DESIGN			MODEL	SMS 1460	
DETAIL			SCALE	NONE	
CHECK			DRAW	MDE	3-13-63
APPRD	KLG	4-25-63	CHECK		

DATE	CHANGE NO.	APPROVAL
4-25-63	1168008	
3-13-64	120037	GWS
11-21-64	122721	GLK
3-26-65	123735	GLK
	132174	

DATE	CHANGE NO.	APPROVAL

DEVELOPMENT NO.

734404

C

2-2

734387

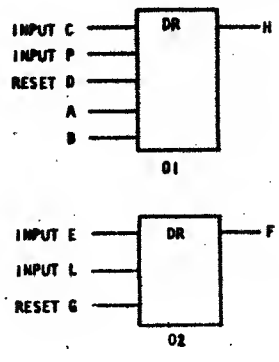
734387

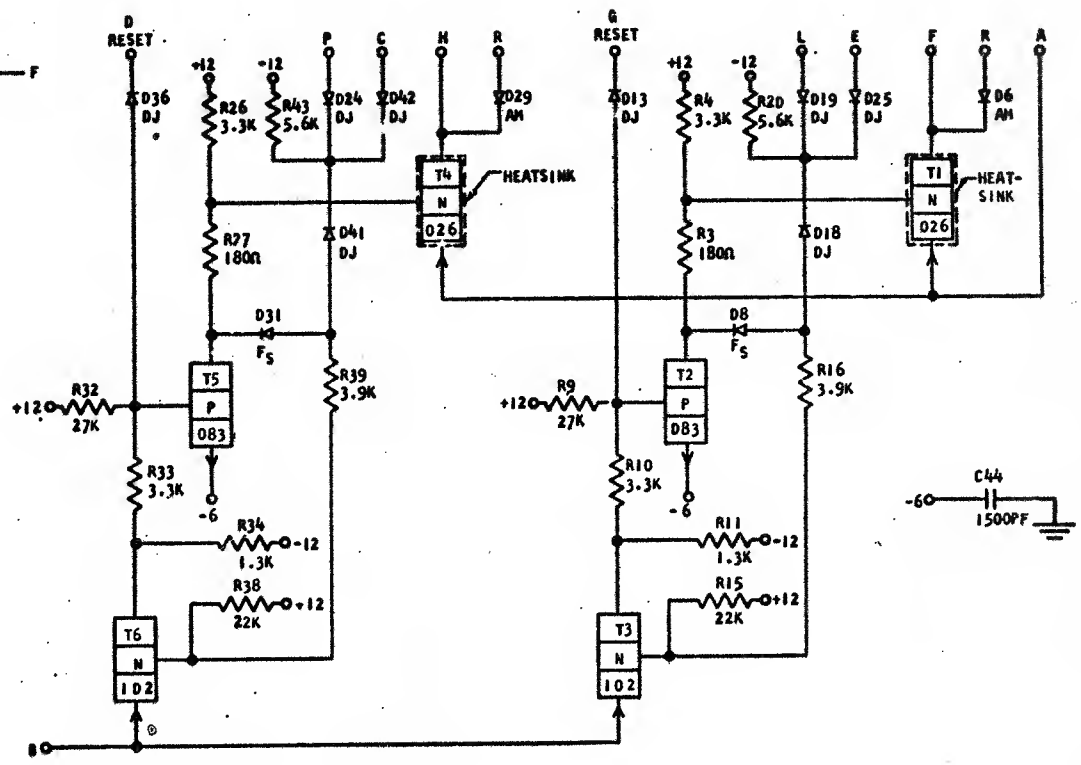
DKJ—

P/N: 372473 EC: 0114747

REFERENCE DRAWING
PRODUCTION DRAWING 372473

SDTDL RELAY DRIVER LATCHING





SEQUENCE OF OPERATION

1. PINS P AND C DOWN: T6 TURNS ON CAUSING T5 TO TURN ON.
2. WHEN T5 TURNS ON T4 ALSO TURNS ON AND CLAMPS THE BASE OF T6 NEGATIVE. THE CIRCUIT IS NOW LATCHED.
3. TO RESET THE LATCH, A NEGATIVE GOING PULSE IS REQUIRED AT PIN D.

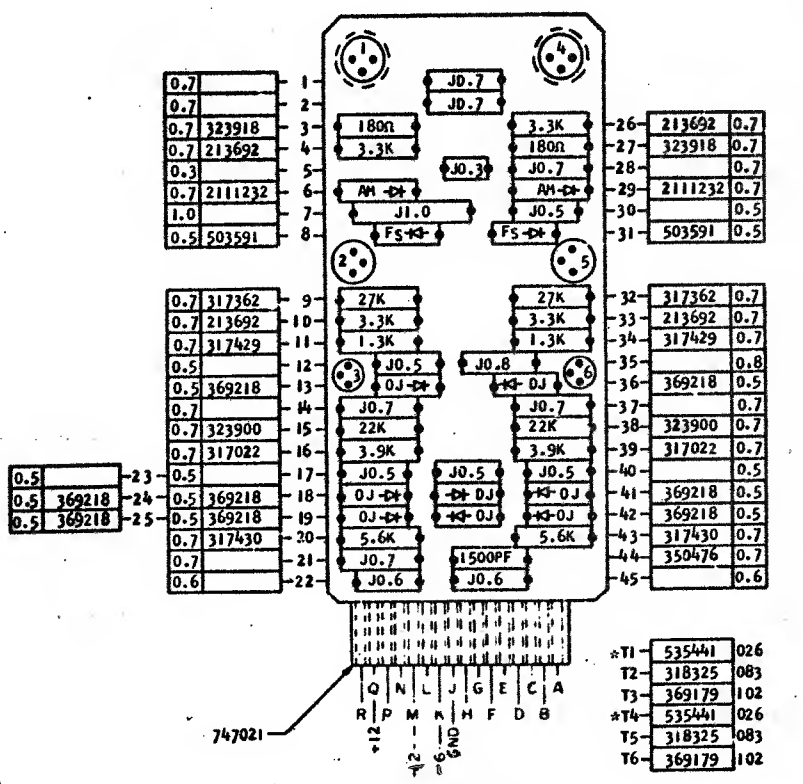
NOTE:
PINS A AND B ARE USUALLY TIED TO GROUND

PINS		SIGNAL NAME	WAVESHAPE		LEVELS MIN	LEVELS MAX
P,L	Y	INPUT		UP	-.65V	+.24V
				DOWN	-5.76V	-12.48V
C,E	Y	INPUT		UP	-.65V	+.24V
				DOWN	-5.76V	-12.48V
D,G	Y	RESET INPUT		UP	-.65V	+.24V
				DOWN	-5.76V	-12.48V
H,F	Y	OUTPUT		UP	-.7V	+.24V
				DOWN	——	—— ☆

☆ DOWN LEVEL DEPENDS UPON THE COLLECTOR RETURN VOLTAGE

DELAY

TURN ON: MAXIMUM OF 800 NSEC
TURN OFF: NOT APPLICABLE



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTOL RELAY DRIVER LATCHING				4-25-63	116800B					734387
DESIGN			MODEL	SMS 1460							
DETAIL			SCALE	NONE							
CHECK			DRAW	MOE 2-20-63							
APPRO		4-25-63	CHECK								

C

2-2

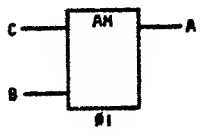
734390

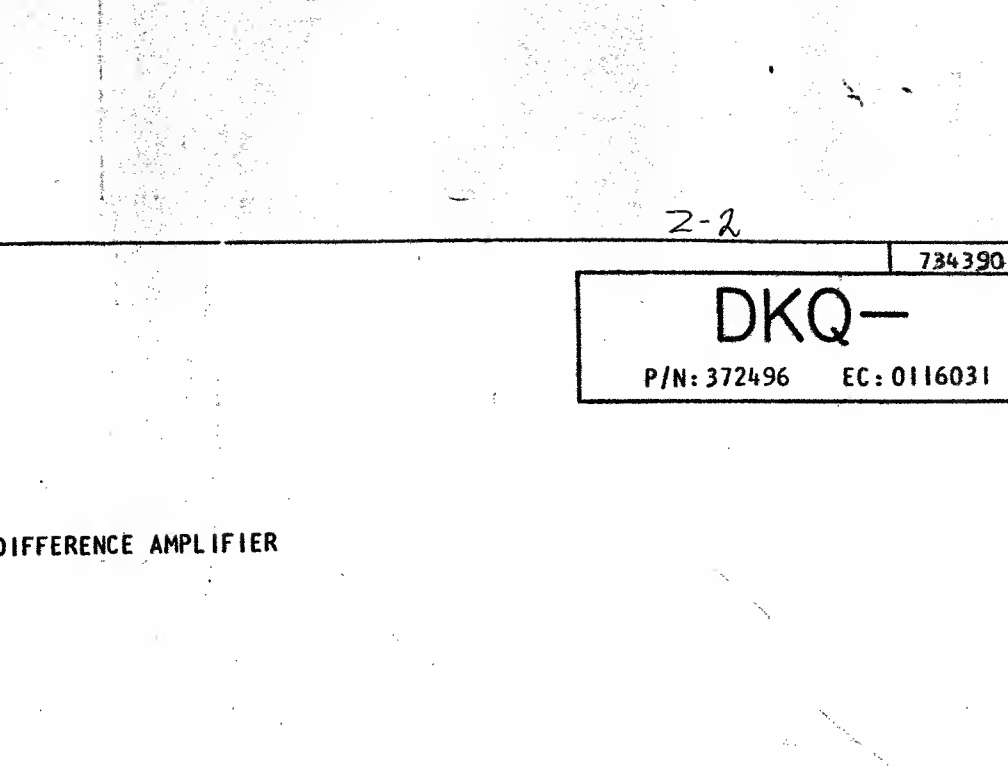
DKQ—

P/N: 372496 EC: 0116031

REFERENCE DRAWING
PRODUCTION DRAWING 372496

DIFFERENCE AMPLIFIER





SEQUENCE OF OPERATION

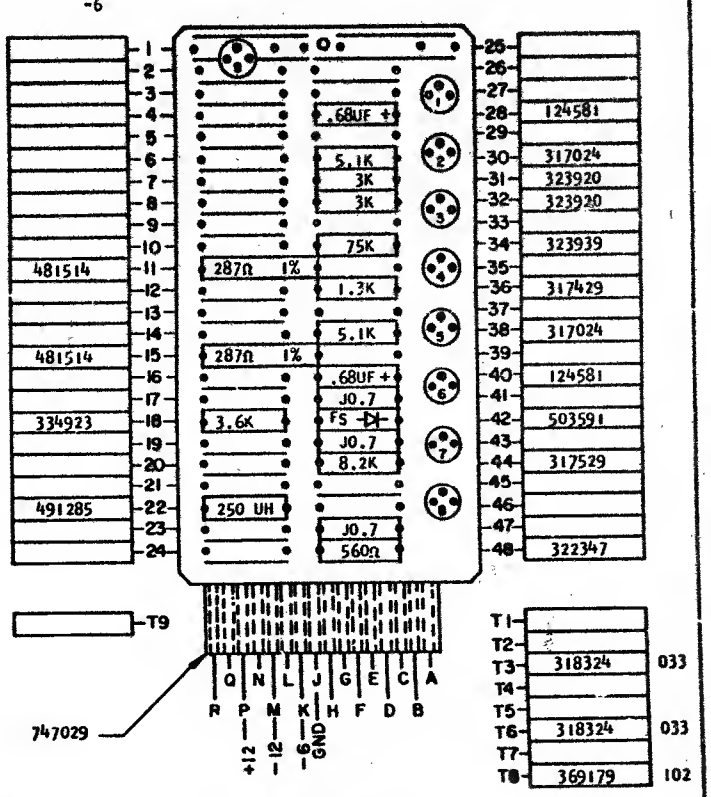
1. WHEN INPUT SIGNALS AT PINS C AND B ARE PASSING THROUGH THE ZERO CROSSOVER POINTS, A PULSE WAVE OUTPUT WILL RESULT.
2. AN UP LEVEL AT THE OUTPUT FROM THE INVERTER IS PRODUCED AT THE ZERO CROSSOVER OF THE INPUT SIGNAL TO SENSE AMPLIFIER STAGE 1 (REFER TO REFERENCE DRAWING WV--)

PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
C	U	INPUT		UP	-5.5V	+.24V
				DOWN	-7.6V	-12.5V
B	U	INPUT		UP	-5.5V	+.24V
				DOWN	-7.6V	-12.5V
A	Y	OUTPUT		UP	-.65V	-.4V
				DOWN	-5.81V	-6.24V

(100 µS/DIV)

DELAY (NSEC)

	MIN	MAX
TURN ON	76	124
TURN OFF	100	900



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734390
NAME	DIFFERENCE AMPLIFIER				4-25-63	116800B						
DESIGN			MODEL	SMS 1460								
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE 2-20-63								
APPRO	RES 4-25-63		CHECK									

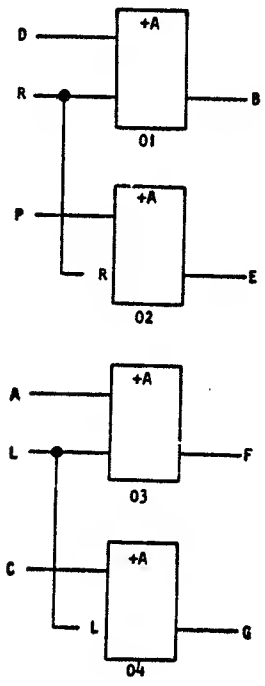
C

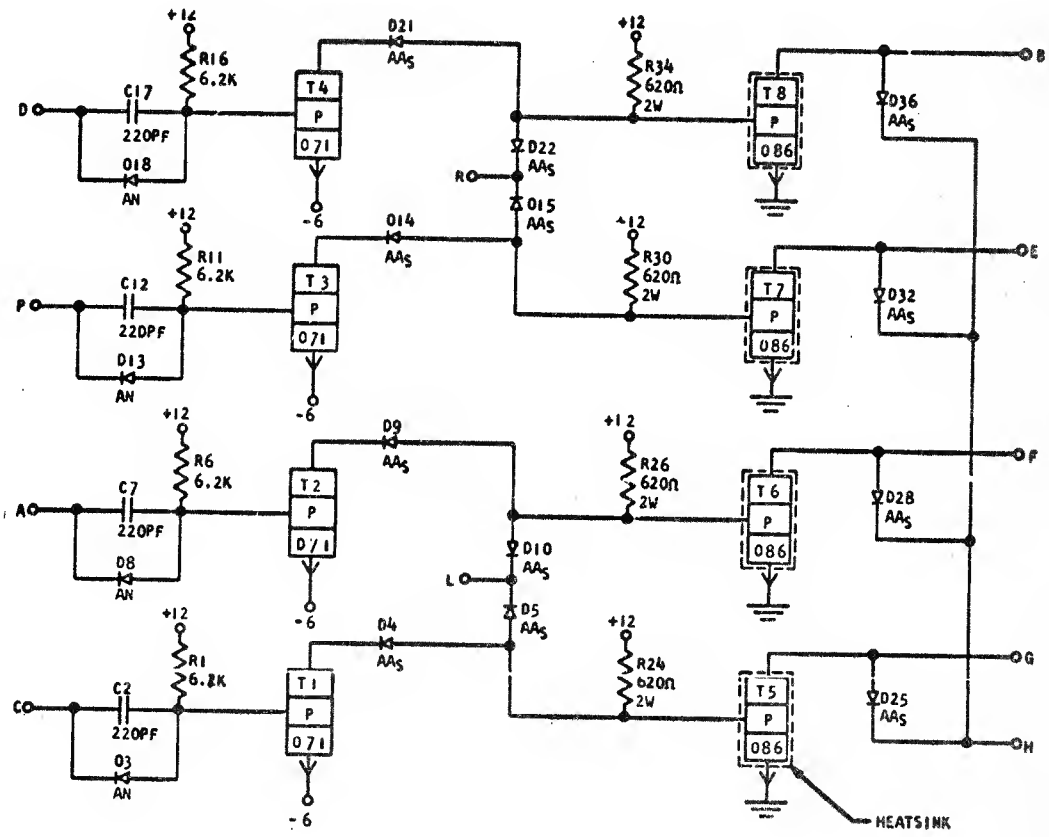
734442

REFERENCE DRAWING
PRODUCTION DRAWING 372497

INHIBIT DRIVER

DKR-
P/N: 372497





SEQUENCE OF OPERATION

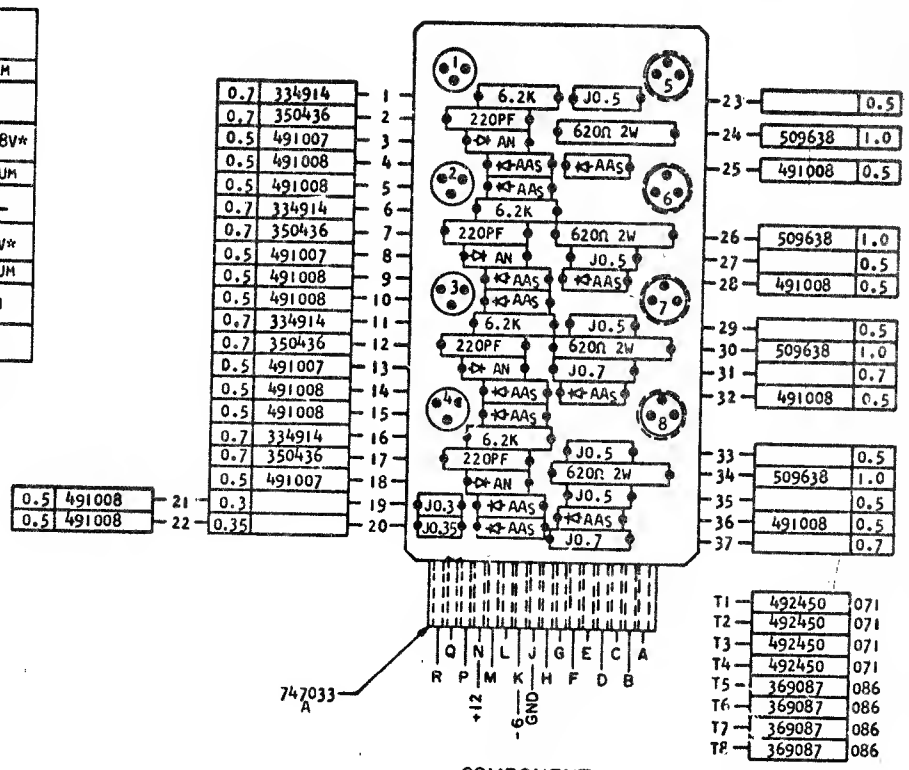
1. IF BOTH INPUTS D AND R ARE UP, TRANSISTOR T4 IS ON, TRANSISTOR T8 IS OFF AND OUTPUT B IS AT THE VOLTAGE LEVEL APPLIED TO PIN H.
2. IF INPUT D IS DOWN AND R IS UP, TRANSISTOR T4 IS OFF, TRANSISTOR T8 IS ON AND OUTPUT B IS AT GROUND LEVEL.

PINS	SIGNAL NAME	WAVESHAPE	LEVELS	MINIMUM	MAXIMUM
D P A C	INPUT		UP	-4.66V	0V
			DOWN	-6.94V	-12.48V*
R L	INPUT			MINIMUM	MAXIMUM
			UP	+1.74V	———
			DOWN	-1.14V	-6.24V*
B E F G	OUTPUT			MINIMUM	MAXIMUM
			UP	NOTE 1	NOTE 1
			DOWN	+0.5V	0V

NOTE 1 - UP LEVEL VOLTAGE VALUE IS THE VOLTAGE APPLIED TO PIN H ± THE SUPPLY TOLERANCE

* - FUNTION OF LOAD

DELAY	MAXIMUM
T_{ON} (N SEC)	900
T_{OFF} (N SEC)	350



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	INHIBIT DRIVER				
DESIGN	REL	8-30-63	MODEL	SMS 1448	
DETAIL	REL	8-30-63	SCALE	NONE	
CHECK	OCK	9-30-63	DRAW	VE	8-27-63
APPRO	OCK	9-30-63	CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
9-27-63	116691					
14OCT65	125832					

734442

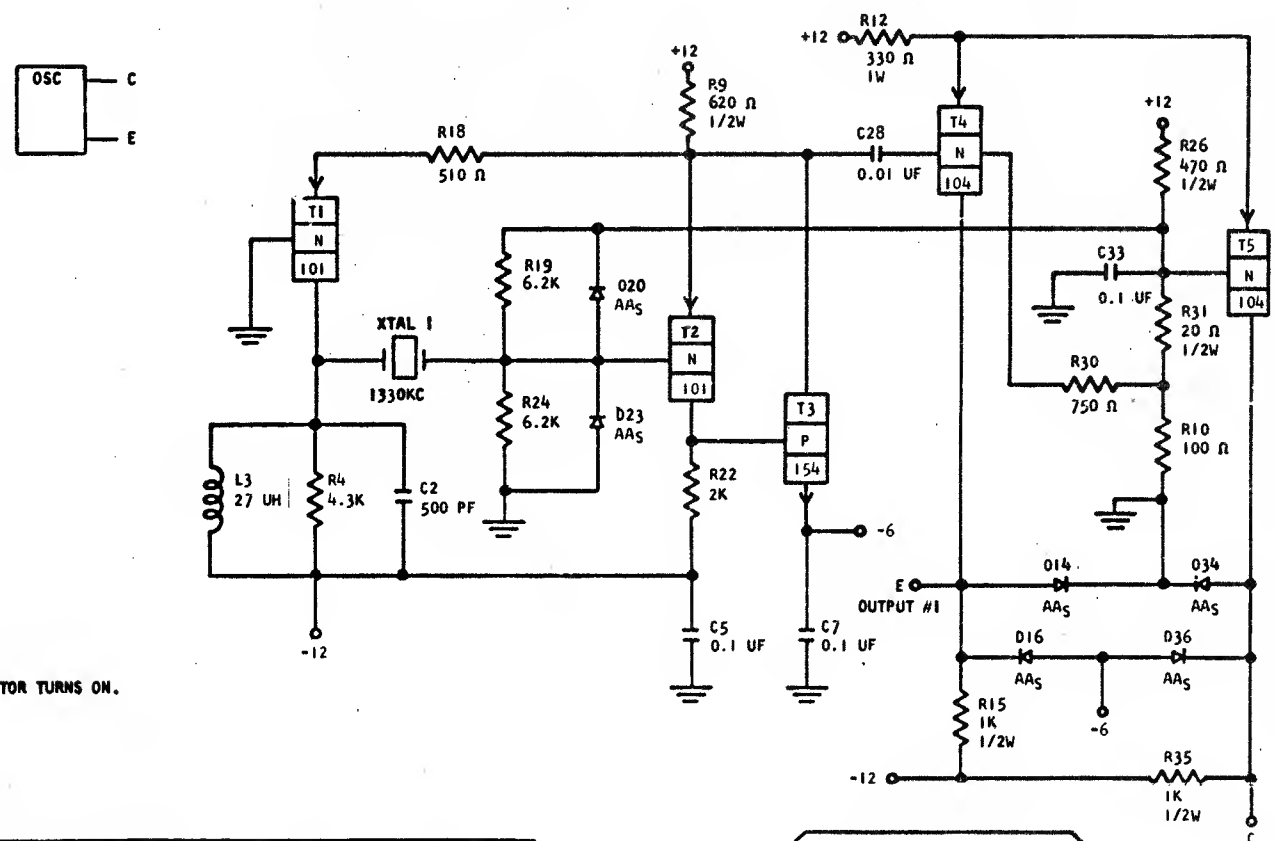
2-1

CARD CODE	734373
DKS-	

734373

REFERENCE DRAWING
PRODUCTION DRAWING 372501

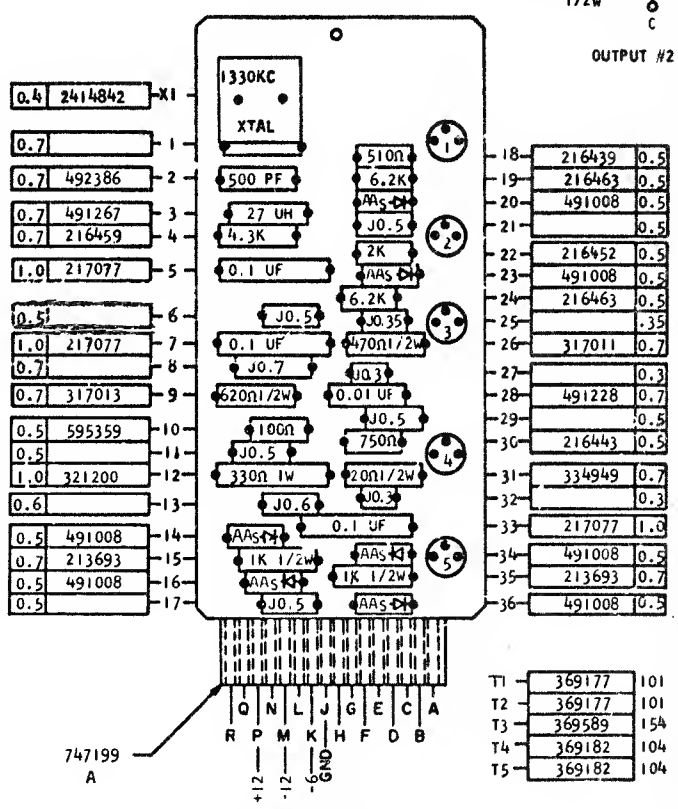
1330 KC OSCILLATOR AND SHAPER



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.

PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
C	Y	OUTPUT #2		UP	0.0V	+0.5V
				DOWN	-5.86V	-6.64V
E	Y	OUTPUT #1		UP	0.0V	+0.5V
				DOWN	-5.86V	-6.64V



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANCE NO.	APPROVAL	DEVELOPMENT NO.	734373
NAME	SDTOL 1330 KC OSCILLATOR AND SHAPER					4-17-63	116800A						
						9-11-63	117848						
DESIGN			MODEL	SMS 1440		12-29-64	120699	GLK					
DETAIL			SCALE	NONE		140CT65	125832					CIRCUIT FAMILY SOTOL	
CHECK			DRAW	ARP 8-23-63									
APPRD			CHECK	[illegible] 8-23-63									

C

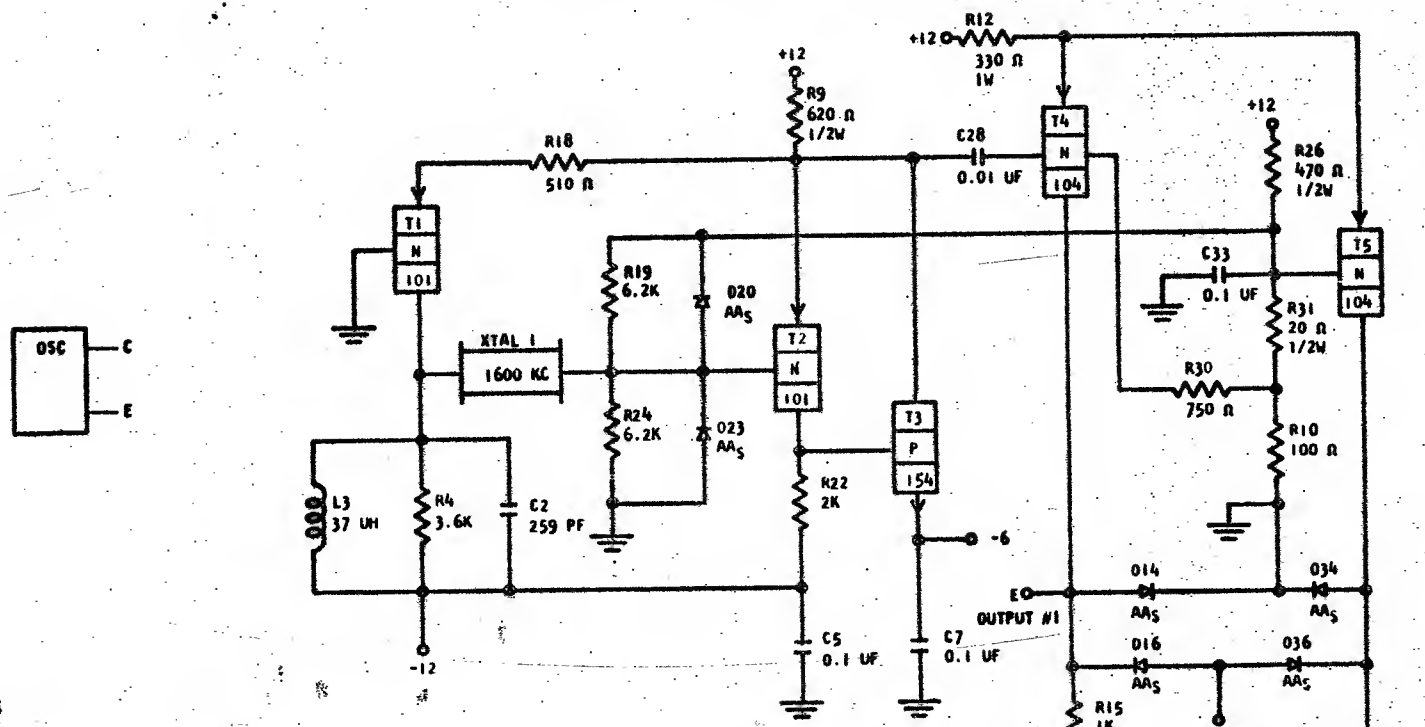
2.

CARD CODE	734372
D K T -	

734372

REFERENCE DRAWING
PRODUCTION DRAWING 372500

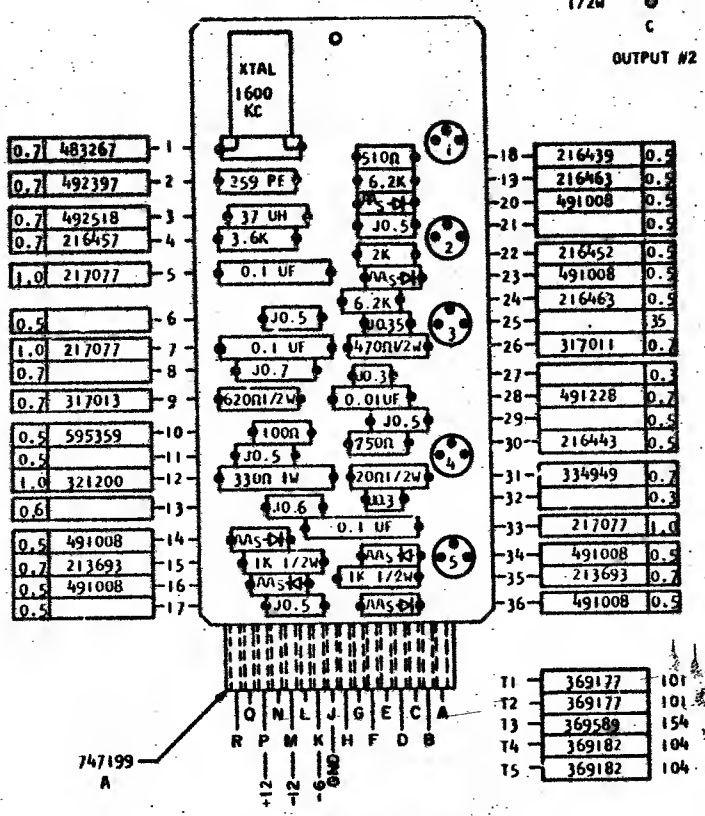
1660 KC OSCILLATOR AND SHAPER



SEQUENCE OF OPERATION

1. WHEN POWER IS UP. THE OSCILLATOR TURNS ON.

PINS		SIGNAL NAME	WAVESHAPE		LEVELS MIN	LEVELS MAX
C	Y	OUTPUT #2		UP	0.0V	+0.5V
				DOWN	-5.86V	-6.64V
E	Y	OUTPUT #1		UP	0.0V	+0.5V
				DOWN	-5.86V	-6.64V



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734372
NAME	SDTDL 1600 KC OSCILLATOR AND SHAPER			4-25-63	116800B						
				9-11-63	117848						
DESIGN		MODEL	SMS 1460	140C765	125832						
DETAIL		SCALE	NONE							CIRCUIT FAMILY	
CHECK		DRAW	RP 8-23-63							SDTDL	
APPRD		CHECK	8-23-63								

C

2-2

734420

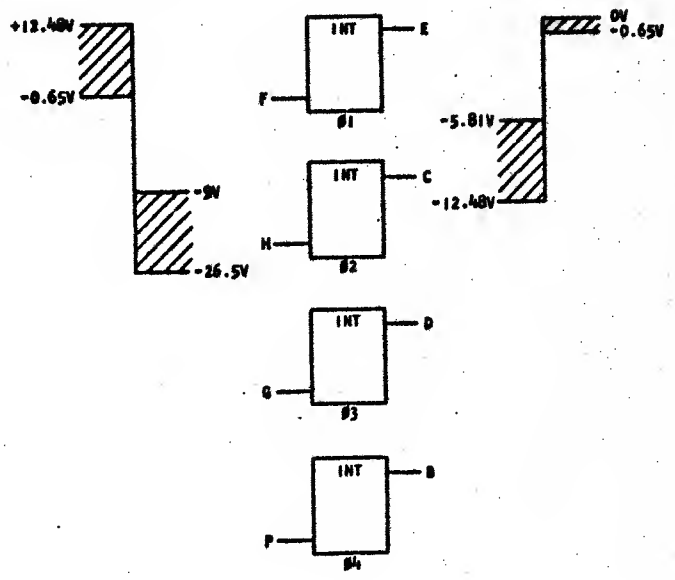
DKU—

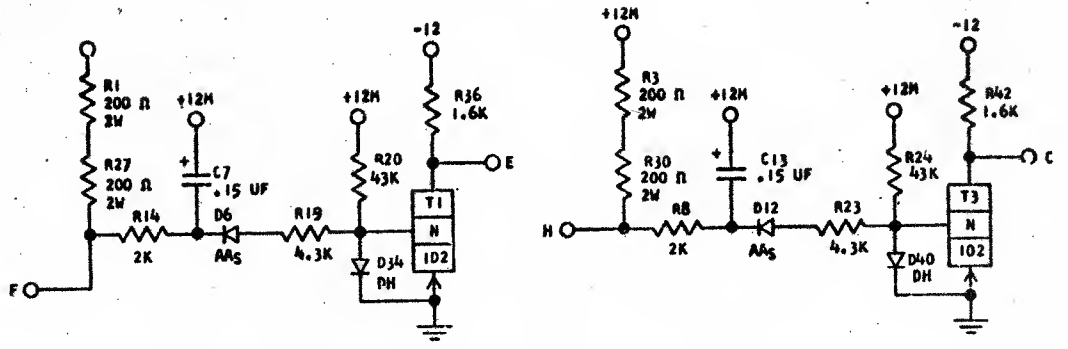
P/N: 372508 EC: 0116056

734420

REFERENCE DRAWING
PRODUCTION DRAWING 372508

SDTDL INTEGRATOR



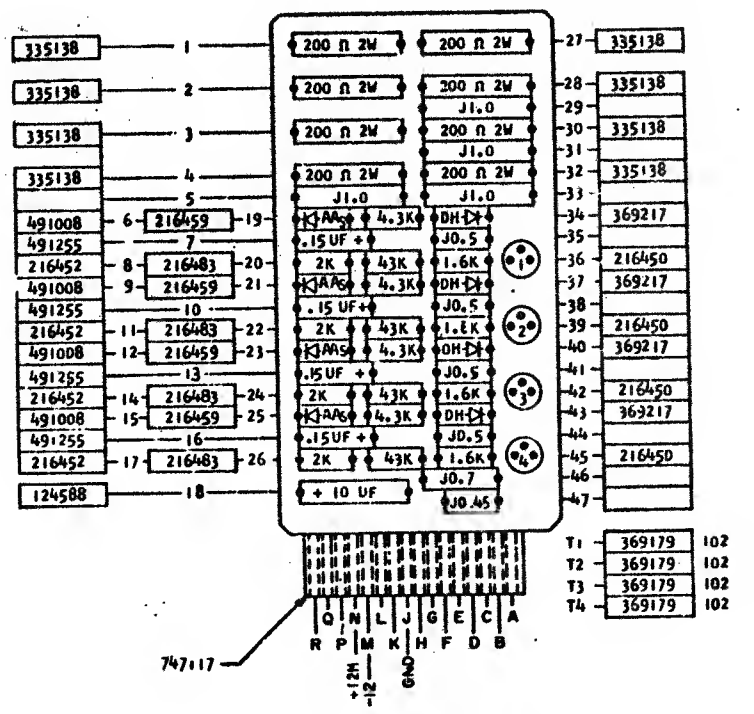


SEQUENCE OF OPERATION

1. INPUT UP: TRANSISTOR OFF, OUTPUT DOWN
2. INPUT DOWN: TRANSISTOR ON, OUTPUT UP

DELAY

	MIN	MAX
T_{ON} (μSEC)	230	350
T_{OFF} (μSEC)	100	122



C

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734420
NAME SDTDL INTEGRATOR					3-25-63	116800						
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE 3-13-63								
APPRO		3-25-63	CHECK									

734376

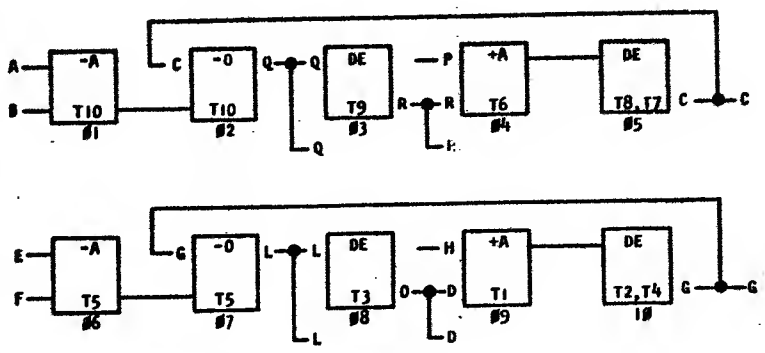
734376

DKW—

P/N: 372526

REFERENCE DRAWING
PRODUCTION DRAWING 372526

SDTDL HS POWER LATCH



OTHER DESIGNATIONS

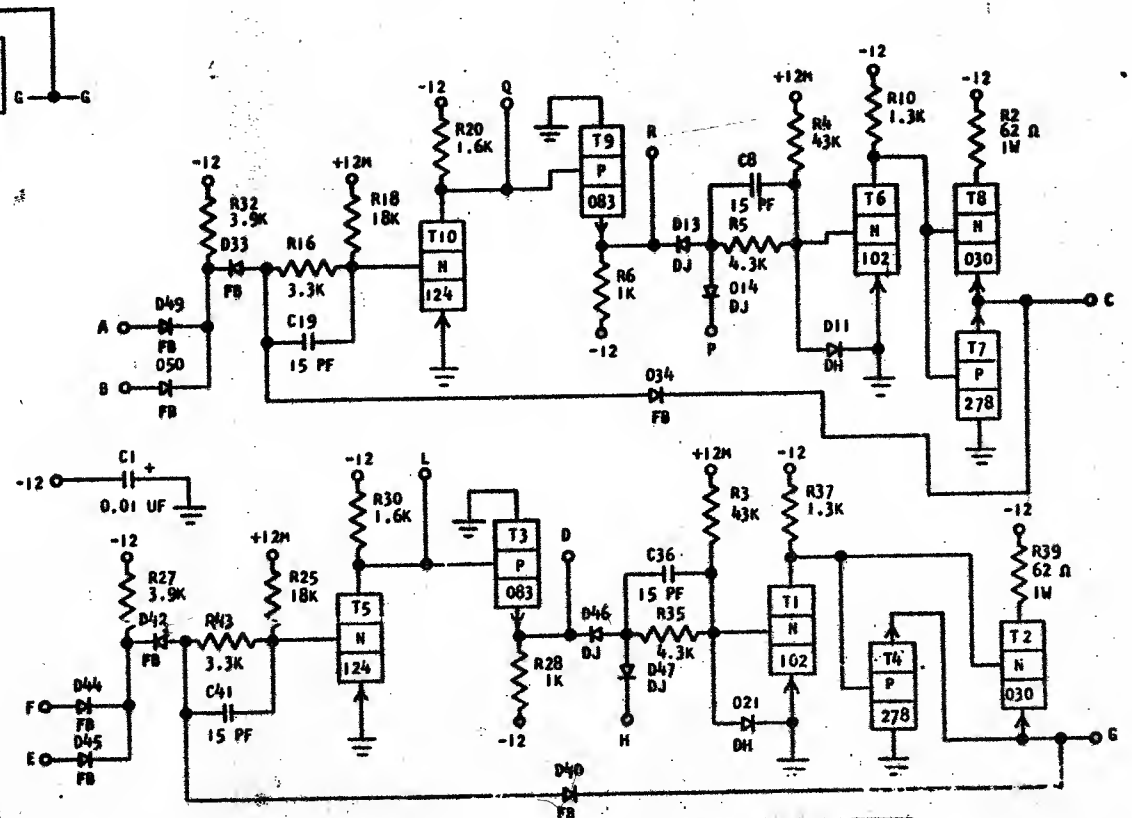
CONF. 1, 6 +O
CONF. 2, 7 +A, -O, +AA
CONF. 4, 9 -O

SEQUENCE OF OPERATION

1. THE FIRST SET OF DIODES TO T10 AND T5 PERFORM A NEGATIVE AND FUNCTION AND THE SECOND SET A NEGATIVE OR.
2. THE LATCH OPERATION IS PERFORMED BY COUPLING THE OUTPUT OF T7 AND T8 BACK TO THE NEGATIVE OR OF T10 AND THE OUTPUT OF T2 AND T4 BACK TO THE NEGATIVE OR OF T5.
3. WHEN THE OUTPUT IS DOWN THE CIRCUIT LATCHES BACK AND HOLDS T5 OR T3 ON UNTIL THE CIRCUIT IS RESET.

NOTE

THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF THE BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.

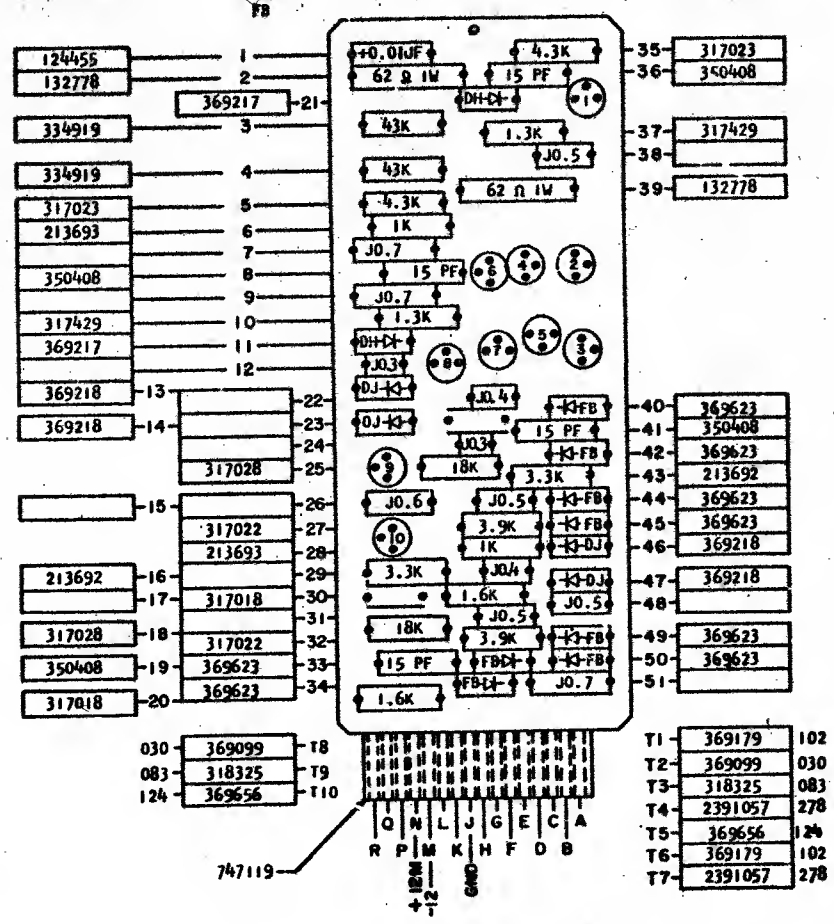


PINS	SIGNAL NAME		WAVESHAPE		LEVELS MIN	LEVELS MAX
A,E	Y	INPUT		UP	-.65V	-.1V
				DOWN	-5.28V	-12.48V
B,F	Y	INPUT	SET	UP	-.65V	-.1V
				DOWN	-5.28V	-12.48V
L,Q	Y	OUTPUT	STORAGE	UP	-0.35V	-.1V
				DOWN	-5.81V	-12.48V
R,D	Y	OUTPUT	STORAGE	UP	-1.10V	-.22V
				DOWN	-5.83V	-7.30V
P,H	Y	INPUT	RESET	UP	-.65V	-.05V
				DOWN	-5.5V	-8.8V
C,G	Y	OUTPUT	STORAGE	UP	-1.25V	-.05V
				DOWN	-6.71V	-6.71V*

* FUNCTION OF I_C

DELAY - NSEC

		MIN	MAX
PINS A, B, E OR F TO PINS Q OR L	TURN ON	15	280
	TURN OFF	24	300
PINS Q OR L TO PINS R OR D	TURN ON	6	20
	TURN OFF	6	28
PINS P, R, H OR D TO PINS C OR G	TURN ON	51	76
	TURN OFF	62	132



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734376
NAME	SDTOL HS POWER LATCH				4-24-63	116800C						
					11-21-64	122721	GLK					
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE 2-8-63								
APPRO	[illegible] 4-24-63		CHECK									

C

734377

2-

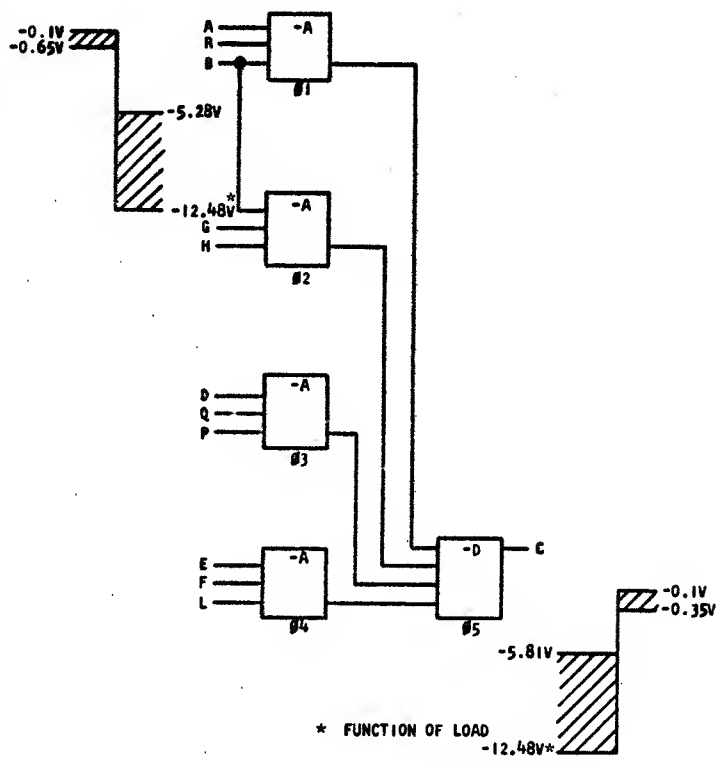
734377

DKX-

P/N: 372527 EC: 0116156

REFERENCE DRAWING
PRODUCTION DRAWING 372527

SDTDL HS FOUR 3-WAY NEGATIVE AND - NEGATIVE OR LOGIC BLOCK WITHOUT LOAD



OTHER DESIGNATIONS

CONF. 1-4 +0
CONF. 5 +A, -00, +AA, -0A, +A0

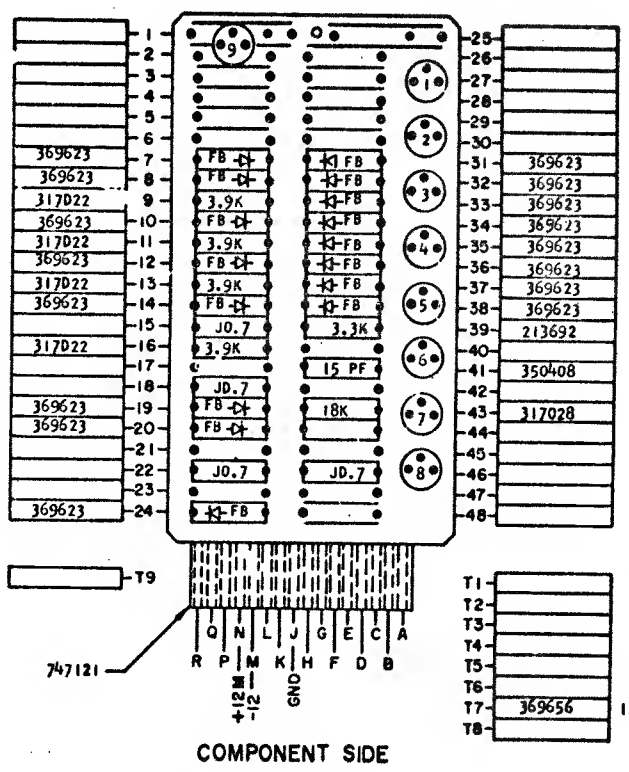
SEQUENCE OF OPERATION

1. PINS F, E AND L MUST BE DOWN TO HAVE A DOWN LEVEL AT D12.
2. PINS D, Q AND P MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
3. A DOWN LEVEL AT D8, D10, D12 OR D14 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER F, E OR L UP WILL CAUSE AN UP LEVEL AT D12.
5. EITHER D, Q OR P UP WILL CAUSE AN UP LEVEL AT D14.
6. THE LEVELS AT D8, D10, D12 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	15	280
TURN OFF (NSEC)	24	300



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME SDTDL HS FOUR 3-WAY NEG AND-NEG OR LOGIC BLOCK WITHOUT LOAD					4-24-63	116800C					734377
DESIGN			MODEL	SMS 1440							
DETAIL			SCALE	NONE							
CHECK			DRAW	MDE 2-8-63							
APPRO		4-24-63	CHECK								

C

2-1

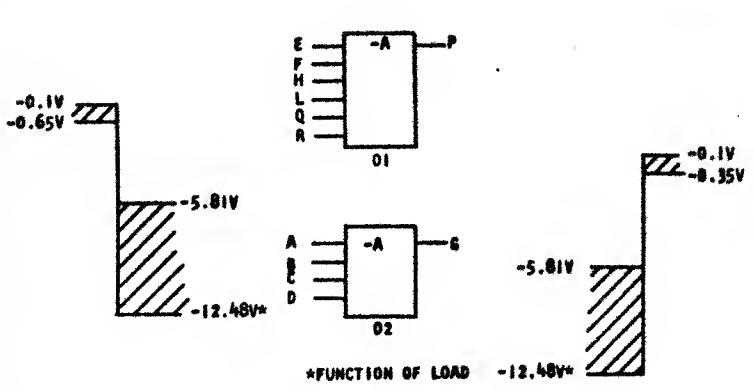
734378

STANDARD CODE 2-7045

LAND CODE DKY- 734378

REFERENCE DRAWING
SEE PRODUCTION DRAWING 372528

HS ONE 6-WAY, ONE 4-WAY NEGATIVE AND LOGIC BLOCKS WITHOUT LOADS



*FUNCTION OF LOAD

OTHER DESIGNATIONS

+0, -A0, +0A, +00, I, I0, IA

SEQUENCE OF OPERATION

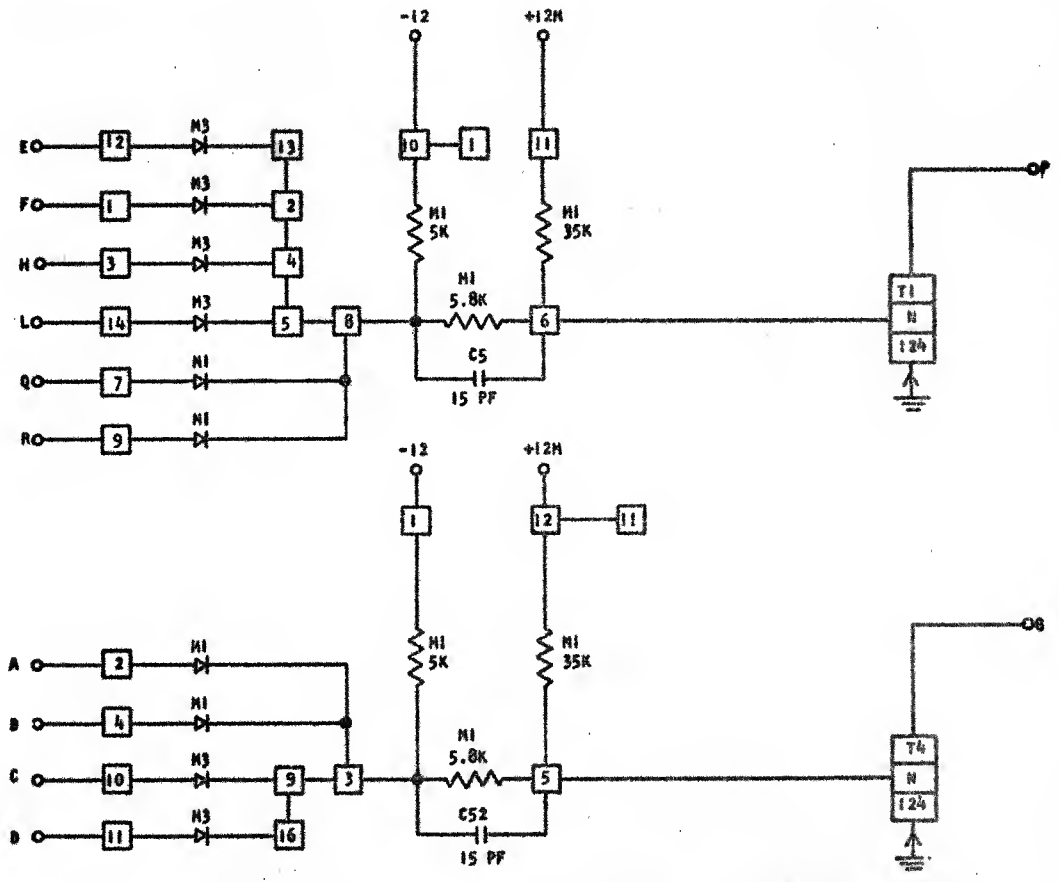
1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP

2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN

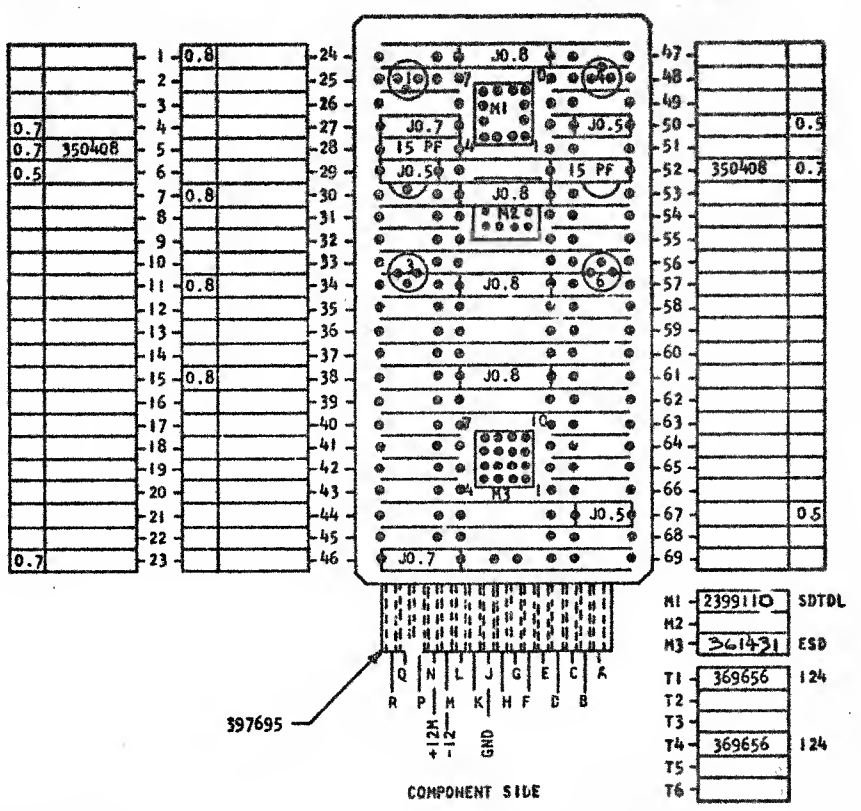
DELAY	MIN	MAX
WITH 560Ω OR 1.6K COLLECTOR RESISTOR		
TURN ON (NSEC)	18	100*
TURN OFF (NSEC)	15	150**

*THIS DELAY CAN INCREASE TO 180 N SEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 200 N SEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734378
NAME	HS 1 6-WAY, 1 4-WAY NEG AND LOGIC BLOCKS WITHOUT LOADS					25APR63	1168008						
DESIGN			MODEL	SMS		30DEC63	119217						
DETAIL			SCALE	NONE			132167						
CHECK			DRAW	LIG	20OCT67							CIRCUIT FAMILY	
APPRO			CHECK									SDTDL	

C

734379

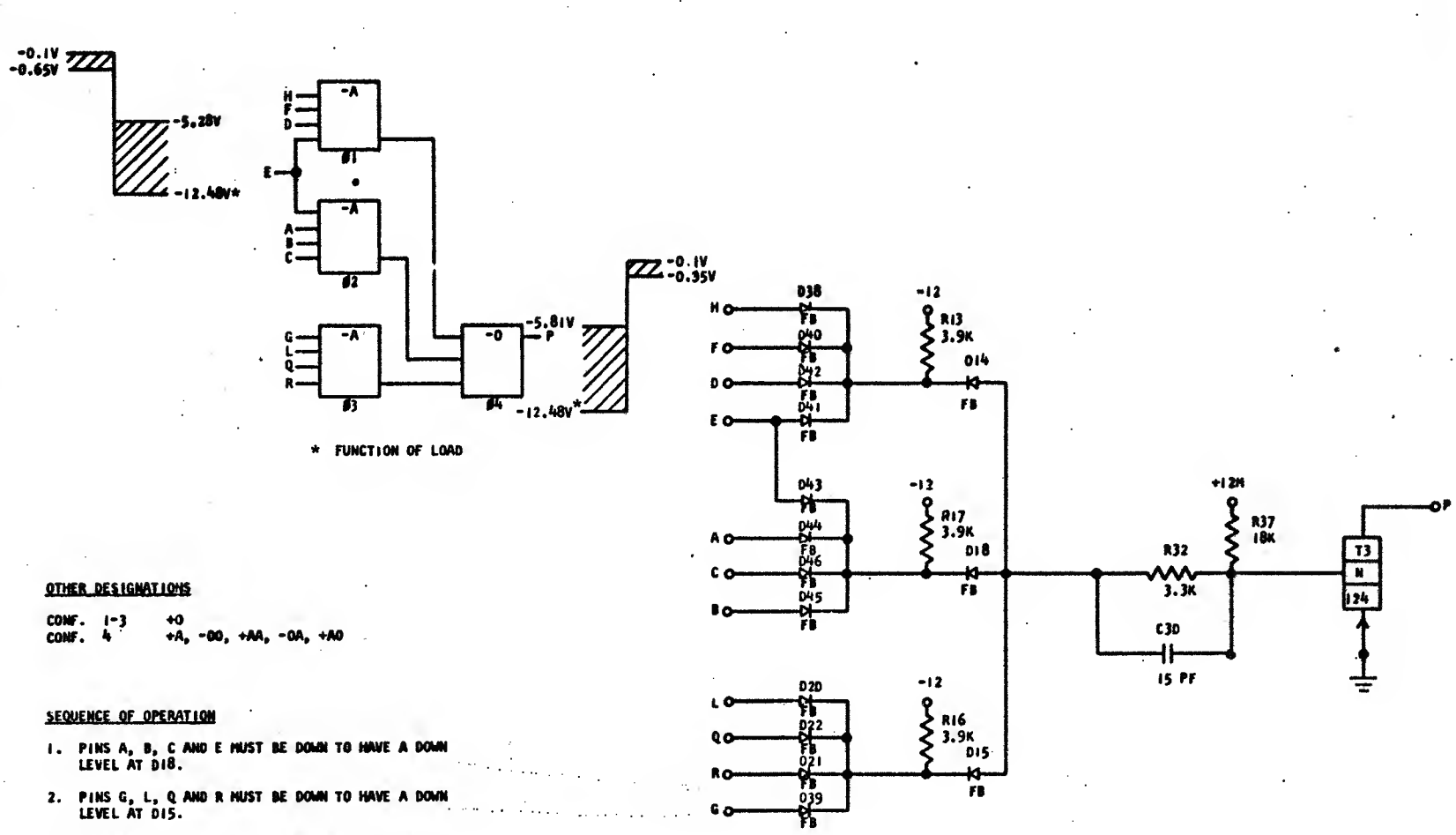
734379

DKZ—

P/N: 372529 EC:0116156

REFERENCE DRAWING
PRODUCTION DRAWING 372529

SDTDL HS THREE 4-WAY NEGATIVE AND - NEGATIVE OR LOGIC BLOCKS WITHOUT LOADS



OTHER DESIGNATIONS

CONF. 1-3 +0
CONF. 4 +A, -00, +AA, -0A, +A0

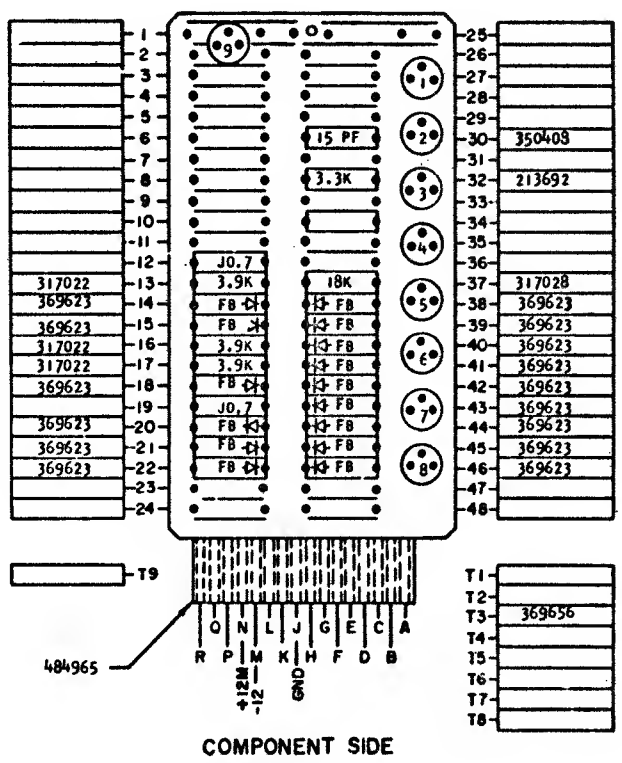
SEQUENCE OF OPERATION

1. PINS A, B, C AND E MUST BE DOWN TO HAVE A DOWN LEVEL AT D18.
2. PINS G, L, Q AND R MUST BE DOWN TO HAVE A DOWN LEVEL AT D15.
3. A DOWN LEVEL AT D14, D15 OR D18 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER A, B, C OR E UP WILL CAUSE AN UP LEVEL AT D18.
5. EITHER G, L, Q OR R UP WILL CAUSE AN UP LEVEL AT D15.
6. THE LEVELS AT D18, D15 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	15	280
TURN OFF (NSEC)	24	300



INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL HS THREE 4-WAY NEG AND -NEG OR LOGIC BLOCKS WITHOUT LOADS					4-24-63	116800C					
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECK			DRAW	MOE	2-8-63							
APPRO	RCA	4-24-63	CHECK									

C

734379

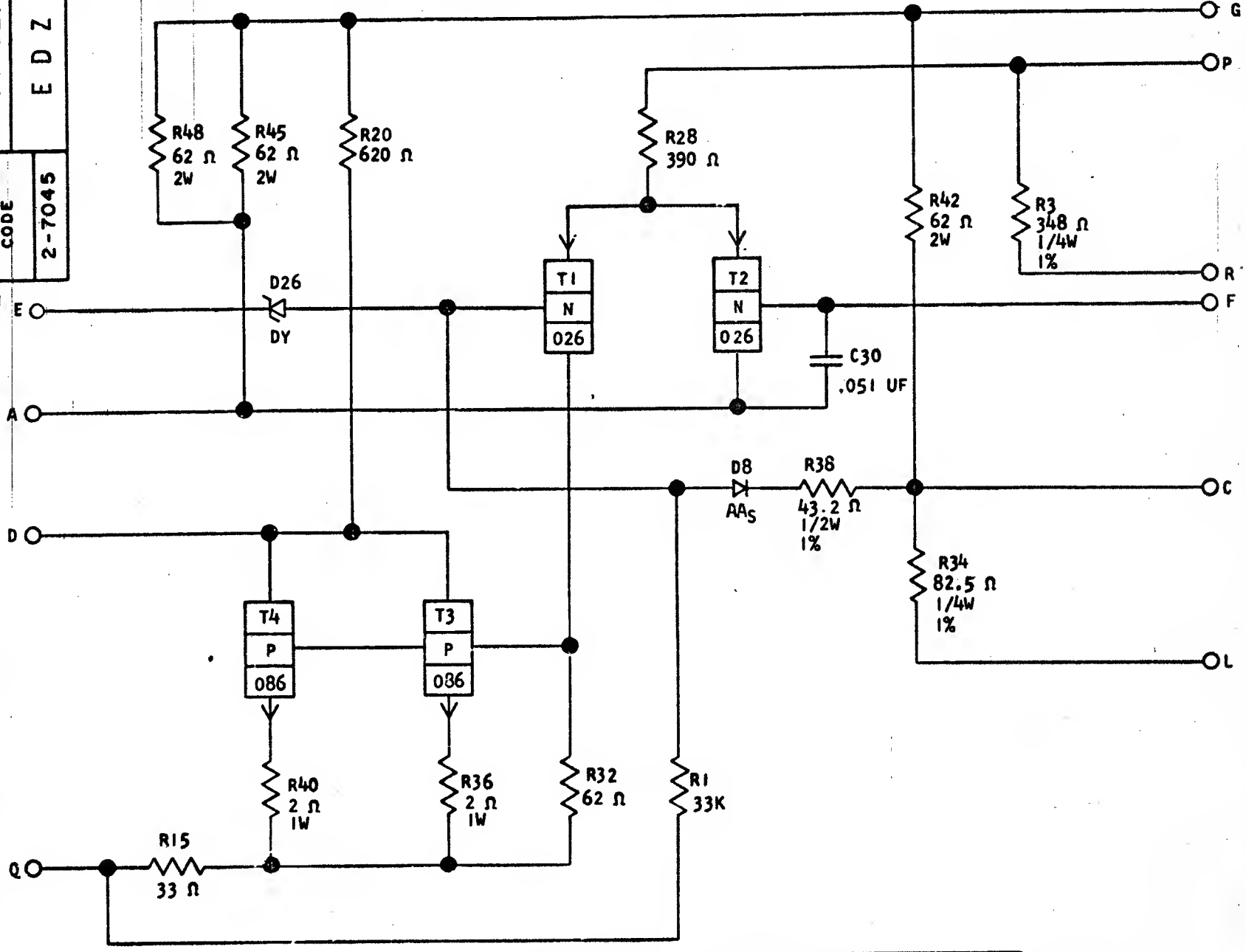
2-1

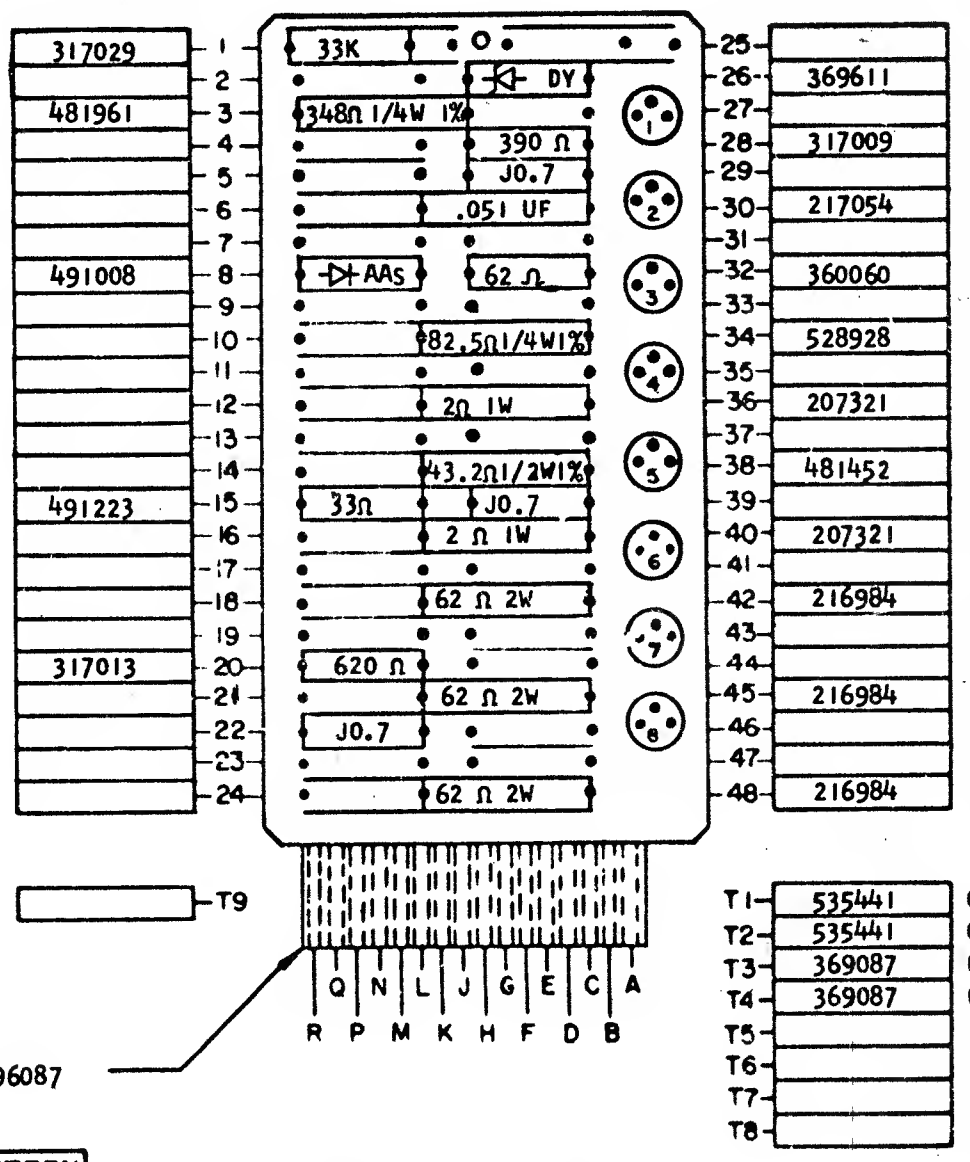
374621

6V AMPLIFIER CARD FOR MPS POWER SUPPLY

374621 EDZ-

STANDARDS CODE 2-7045





NOTES

- X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 893492
- XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
- XII ALL RESISTORS ARE 1/2 WATT AND ± 5% UNLESS OTHERWISE NOTED
- XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296

B

COMPONENT SIDE

DPD CIRCUIT & PACKAGING STANDARD		
APPROVAL	DATE	HOLE PATTERN
GDS	12-11-63	493457

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	374621
NAME	CARD ASM TSTR- 6V AMP					5-21-64	121290	IVL					
CARD FOR MPS POWER SUPPLY													
DESIGN			MODEL	SMS									
DETAIL			SCALE	NONE									
CHECK	JRP	5-21-64	DRAW	HDG	5-3-64								
APPRO	IVL	5-21-64	CHECK	EMS	5-15-64								

2-1

CARD CODE	837973
E S G -	

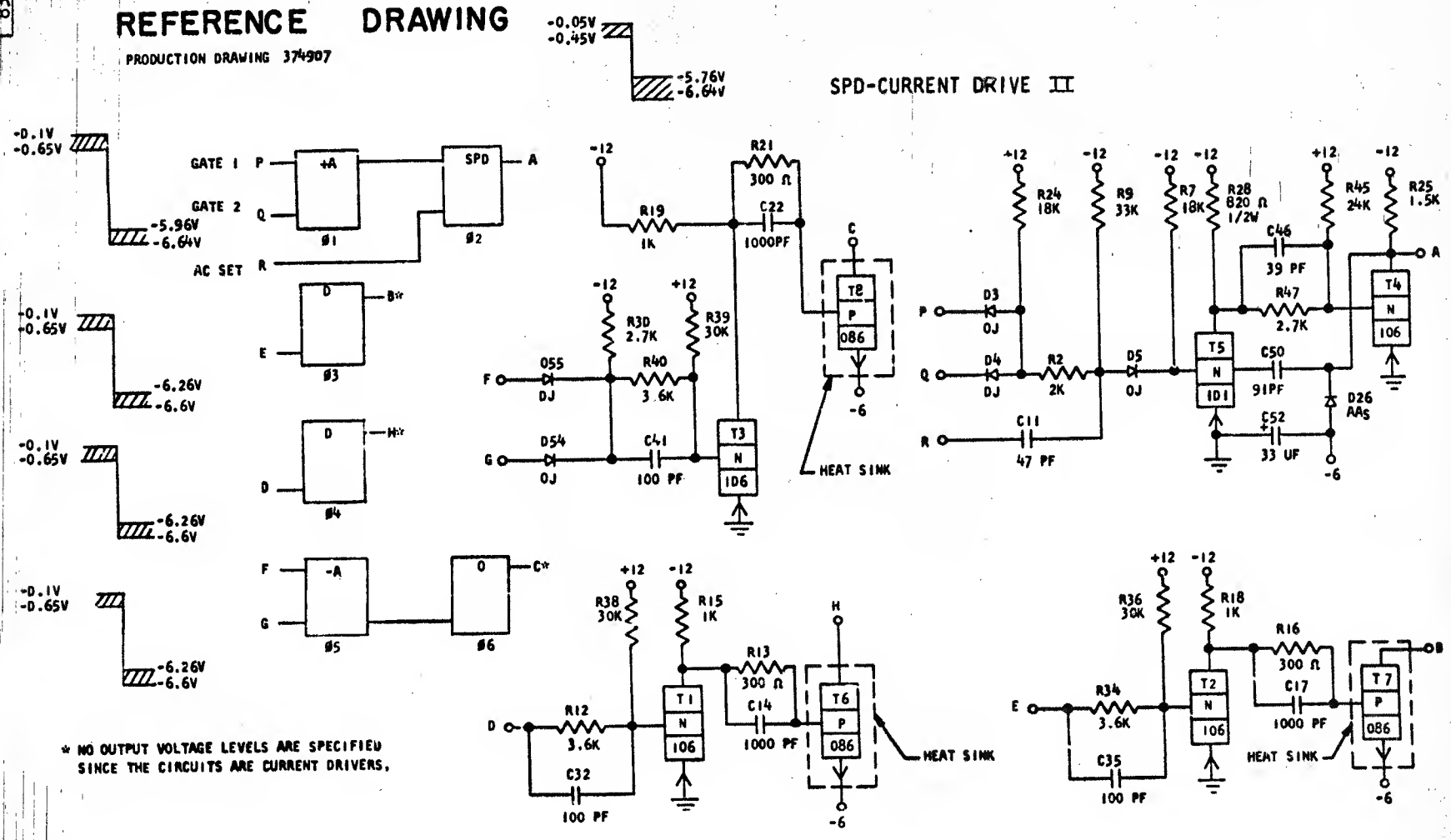
STANDARDS CODE
2-7045

837973

REFERENCE DRAWING

PRODUCTION DRAWING 374907

SPD-CURRENT DRIVE II



* NO OUTPUT VOLTAGE LEVELS ARE SPECIFIED SINCE THE CIRCUITS ARE CURRENT DRIVERS.

OTHER DESIGNATIONS

CONF.	1	D
CONF.	3,4,6	OR
CONF.	5	+0

SEQUENCE OF OPERATIONS:

CONF. 1 AND 2 - SAMPLE PULSE DRIVER

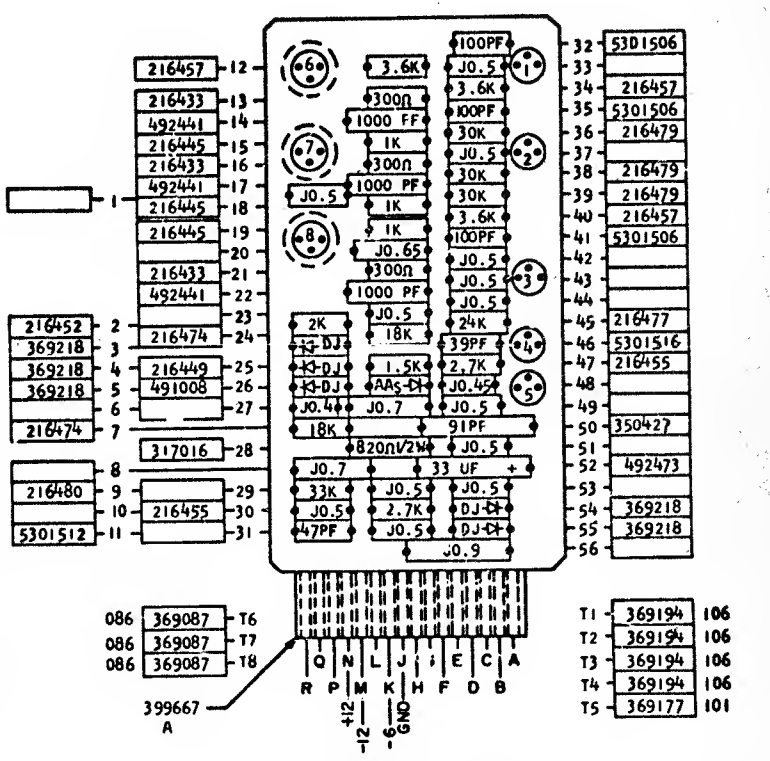
1. INPUTS P AND Q UP CONDITIONS POSITIVE AND INPUT CIRCUIT SO THAT A POSITIVE GOING PULSE ON PIN R TURNS T9 OFF AND T8 ON. OUTPUT IS UP.

   NOTE: THE GATES MUST BE UP FOR AT LEAST 300 NSEC BEFORE AN AC INPUT IS APPLIED. THE GATE AND A-C INPUT RISE TIMES MUST BE 100NS OR LESS IF A 300 NSEC CONDITIONING TIME IS TO BE ACHIEVED. THE AC INPUT SWING MUST NOT EXCEED THE GATE INPUT SWING.

CONF. 3 THROUGH 6 - SET-RESET DRIVER.

1. A DOWN LEVEL ON E OR O OR A DOWN LEVEL ON BOTH PINS F AND G WILL TURN THE DRIVER ON.

DELAY - NSEC		AVERAGE	MAXIMUM
CONF. 1 AND 2	TURN ON	70	75
	TURN OFF	NOT APPLICABLE	
CONF. 3 THRU 6	TURN ON	40	IDD
	TURN OFF	320	625



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
SIZ	3-24-65

INTERNATIONAL BUSINESS MACHINES CORP.														
NAME	SPD - CURRENT DRIVE II													
DESIGN			MODEL	SMS 2821										
DETAIL			SCALE	NONE										
CHECK			DRAW	JAB	3-25-65									
APPRO			CHECK	JD										

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
4-6-65	122304	DRR				
						CIRCUIT FAMILY SDTDL

837973

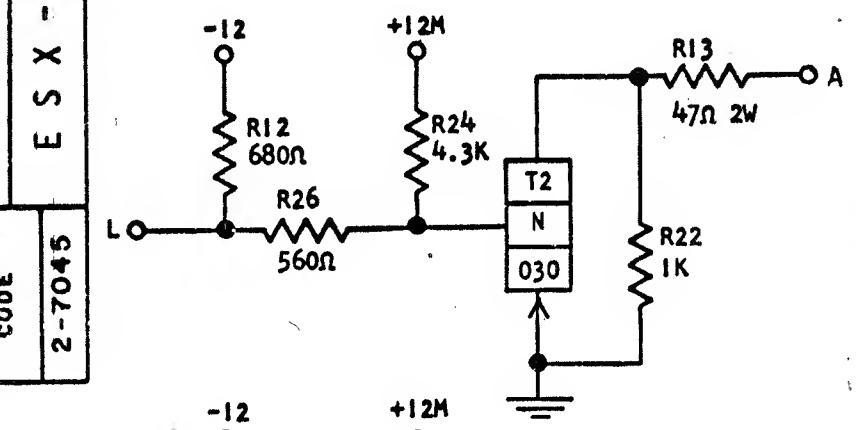
C

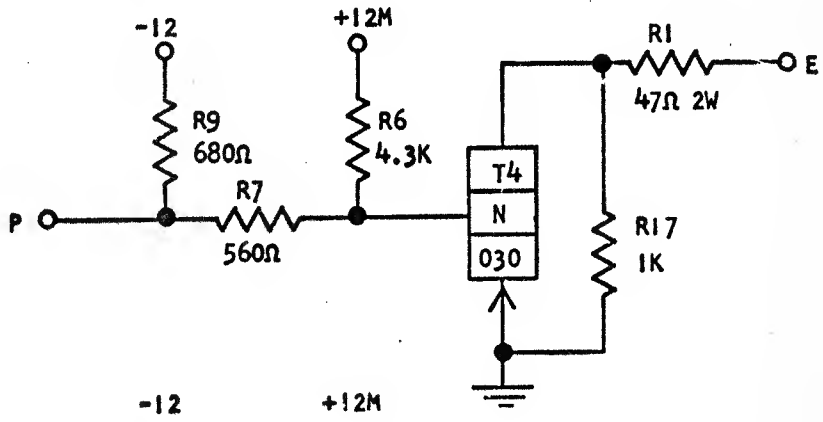
374924

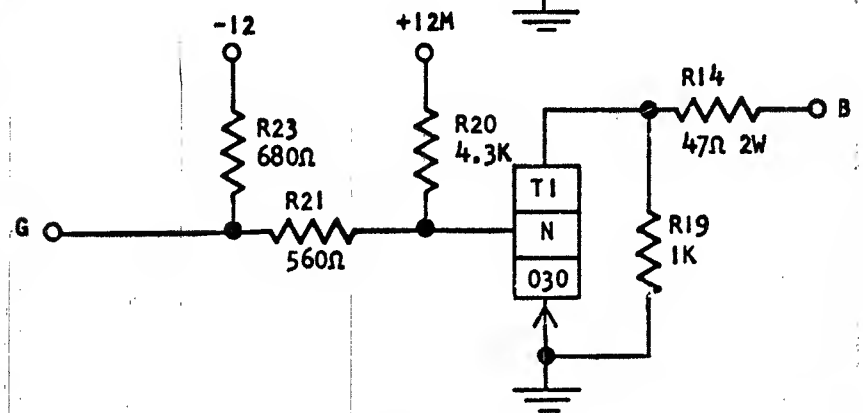
INDICATOR DRIVER

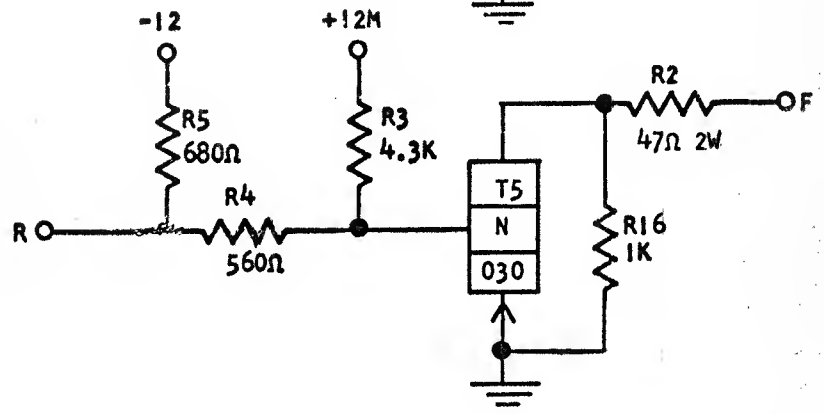
374924 | E S X -

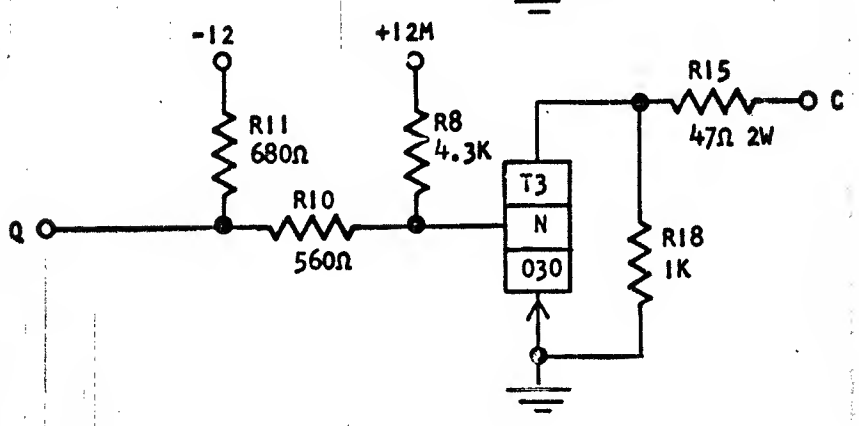
STANDARDS CODE | 2-7045











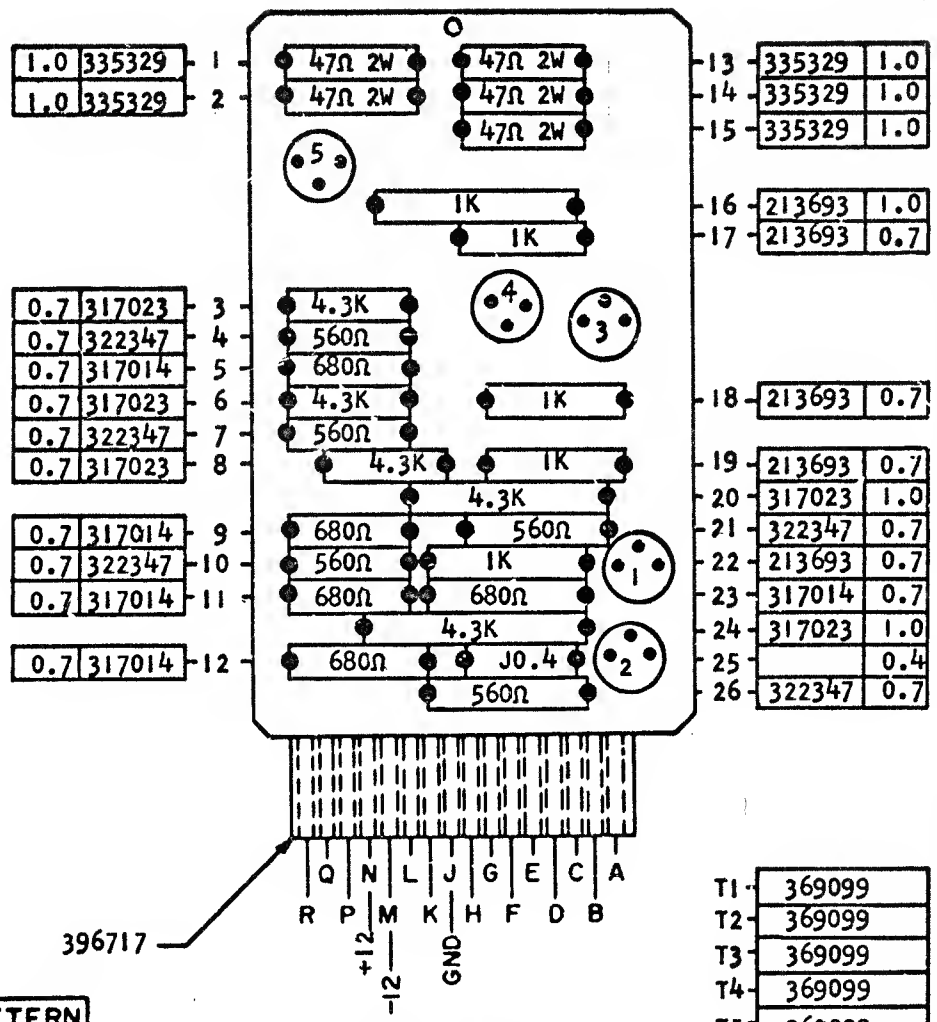
NOTES

X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 893791

XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999

XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED

XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296



T1 369099 030
T2 369099 030
T3 369099 030
T4 369099 030
T5 369099 030

COMPONENT SIDE

B

DPD CIRCUIT & PACKAGING STANDARD		
APPROVAL	DATE	HOLE PATTERN
JHT	2-16-65	396639

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	374924
NAME	CARD ASM TSTR- INDICATOR DRIVER					4-13-65	122312	JHT				PE0117	
DESIGN			MODEL	SMS 2821									
DETAIL			SCALE	NONE									
CHECK	SJ	4-12-65	DRAW	LIG	4-1-65							CIRCUIT FAMILY	
APPRO	JHT	4-12-65	CHECK	SJ	4-7-65							NAND	

C. S.CO., NO. 27BW 41966

849091

849091

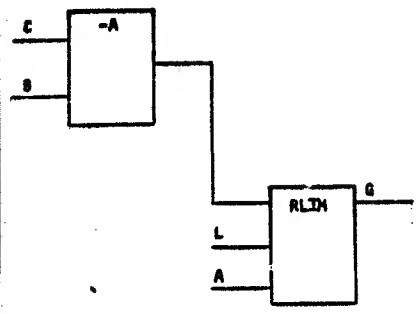
REFERENCE DRAWING
PRODUCTION DRAWING
375157

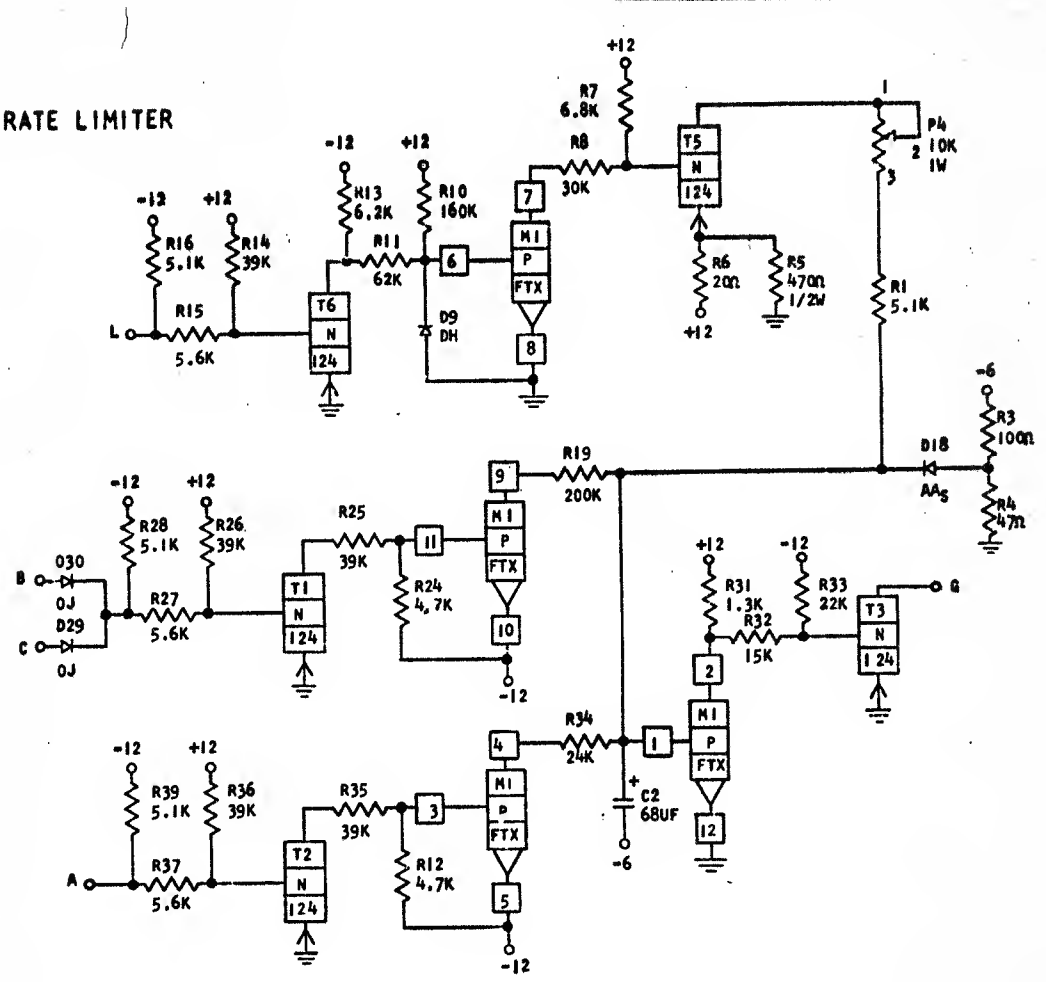
FPZ-

P/N: 375157

STACKER RATE LIMITER

LOGIC SYMBOL

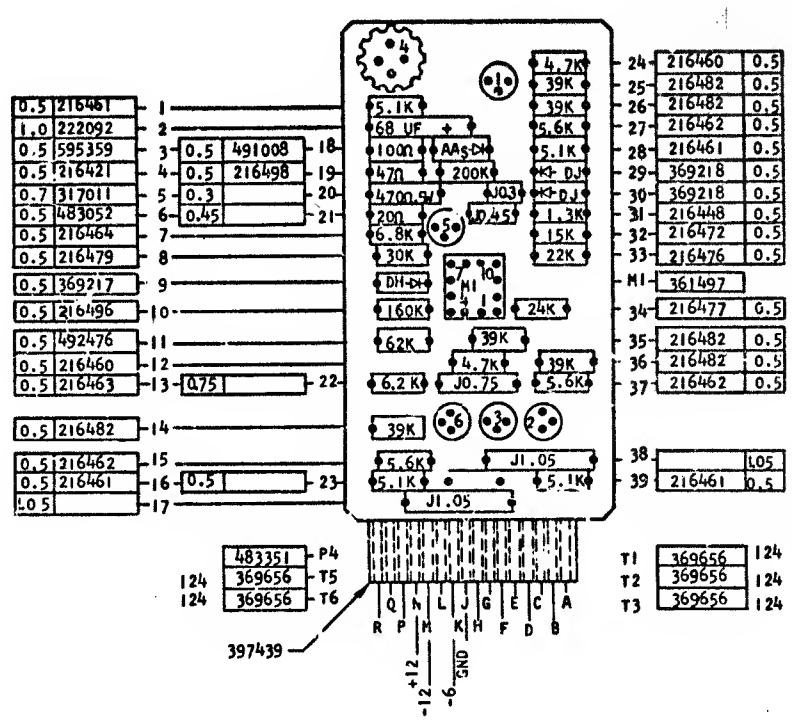




NOTES

1. PIN L INPUT IS AT AN DOWN LEVEL WHEN THE 1403 CARRIAGE IS IN A HIGH SPEED MODE.
2. PINS B AND C ARE AT A DOWN LEVEL WHEN THE PRINTER CARRIAGE IS IN A LOW SPEED MODE.
3. PIN A INPUT IS AT A DOWN LEVEL WHEN THE CARRIAGE IS NOT SPACING.
4. VOLTAGE ON C2 IS AN ANALOGUE OF THE UNSTACKED PAPER STORED IN THE CARRIAGE. WHEN UTILIZED PROPERLY WITH ACCOMPANYING LOGIC THE FOLLOWING SAMPLE SEQUENCE WOULD BE SEEN.

PIN	FUNCTION	WAVEFORM	LEVEL	MAX.	MIN.
L	INPUT		UP	-.1	-.65
			DOWN	-12.48	-5.81.
B,C	INPUT		UP	-.1	-.65
			DOWN	-12.48	-5.81
A	INPUT		UP	-.1	-.65
			DOWN	-12.48	-5.81
G	OUTPUT		UP	-12.48	-5.81
			DOWN	-.1	-.65
C2 VOLTAGE	UNSTACKED PAPER ANALOGUE	THRESHOLD	UP	+.75	+.60
			DOWN	-2.1	-1.8



MFG ENG	PWI	120CT66
CIRCUIT AND PACKAGING STANDARD		
APPROVAL		DATE
S.I.Z.		8SEP66

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASSEMBLY TSTR- STACKER RATE LIMITER					24FEB67	131091					
DESIGN			MODEL	SMS								
DETAIL			SCALE	NONE								
CHECK			DRAW	LIG	20FEB67							
APPRO			CHECK									

849091

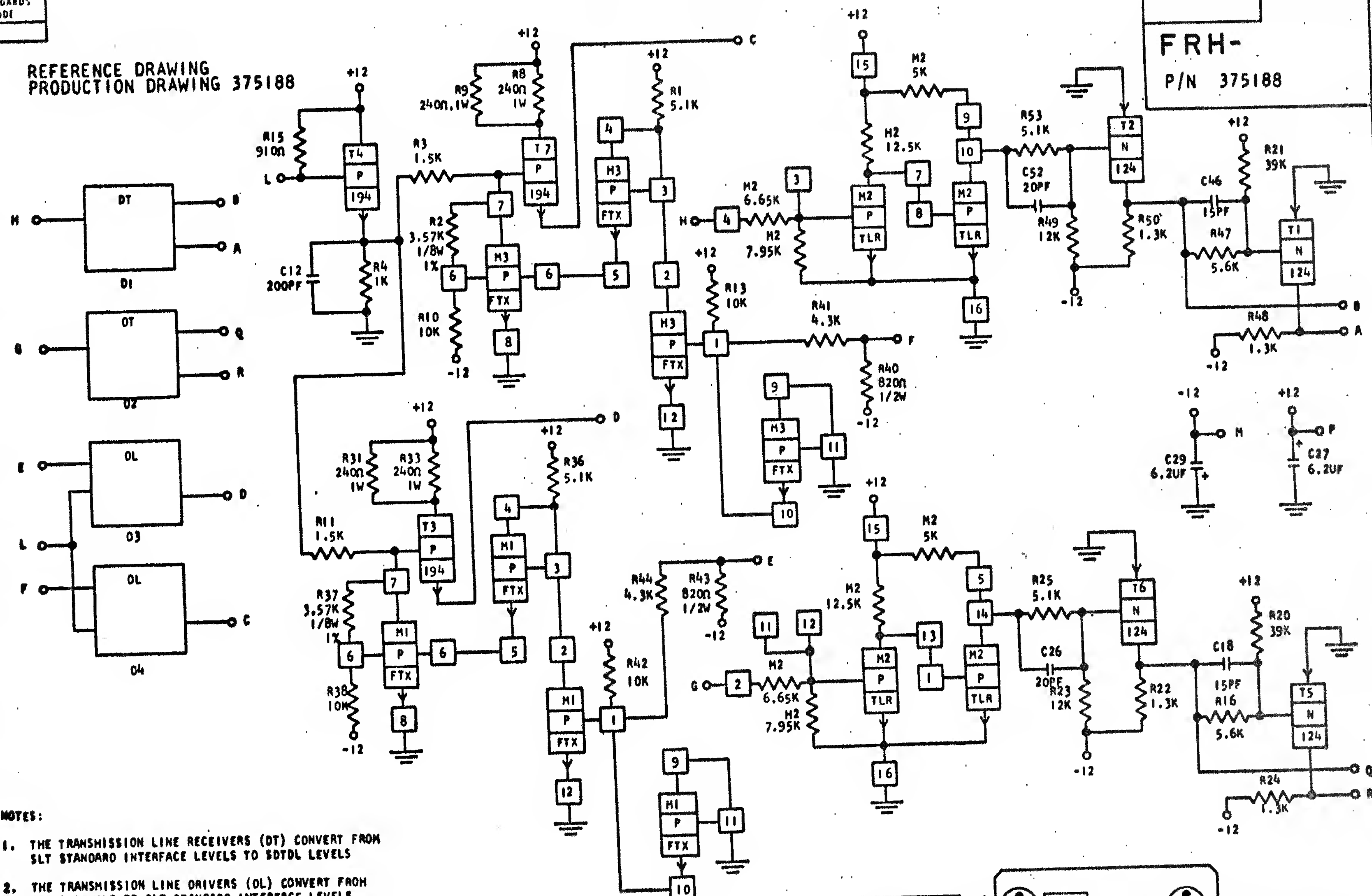
2-1

STANDARDS CODE		CARD CODE	2532396

2532396

REFERENCE DRAWING
PRODUCTION DRAWING 375188

FRH-
P/N 375188



NOTES:

1. THE TRANSMISSION LINE RECEIVERS (DT) CONVERT FROM SLT STANDARD INTERFACE LEVELS TO SDTDL LEVELS

2. THE TRANSMISSION LINE DRIVERS (DL) CONVERT FROM SDTDL LEVELS TO SLT STANDARD INTERFACE LEVELS

SEQUENCE OF OPERATION

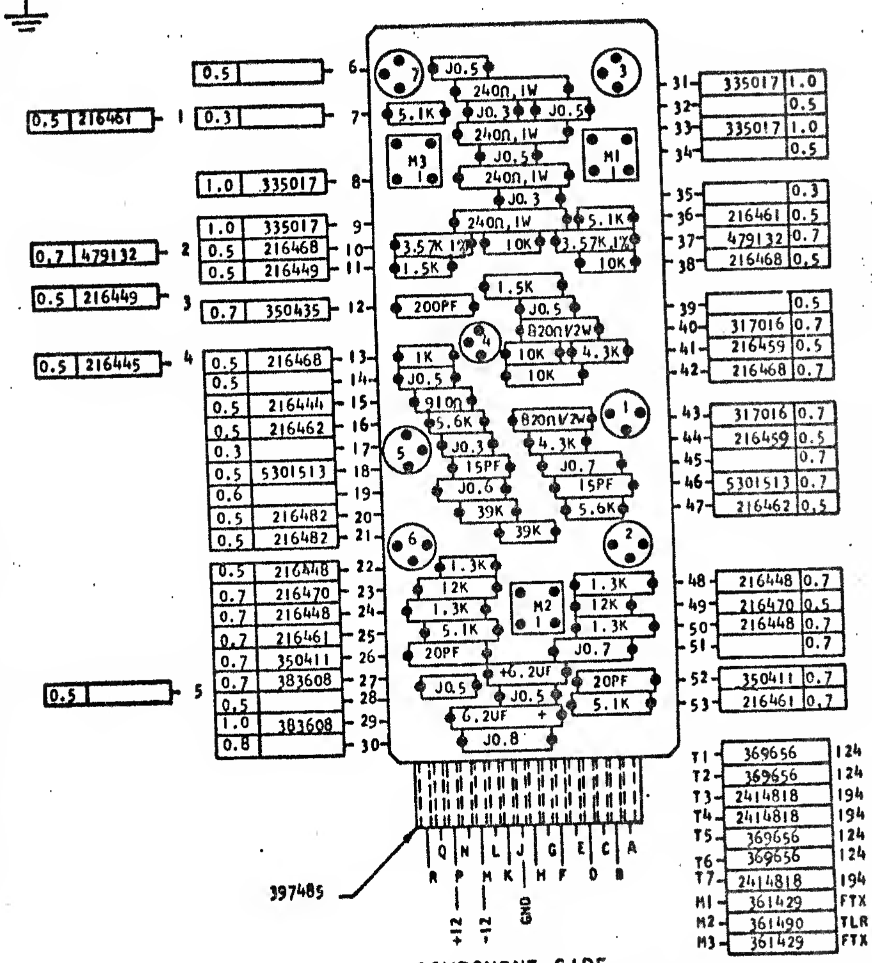
TRANSMISSION LINE RECEIVER (TLR)

1. AN UP LEVEL AT THE INPUT TO THE DT (CONFIGURATION D1, D2) CAUSES AN UP LEVEL AT PINS A AND R AND AN OUT OF PHASE DOWN LEVEL AT PINS B AND Q. A DOWN LEVEL AT THE INPUT CAUSES PINS A AND R TO GO TO A DOWN LEVEL AND PINS B AND Q TO GO TO AN UP LEVEL

TRANSMISSION LINE DRIVER (TLD)

1. AN UP LEVEL AT THE INPUTS TO THE DL (CONFIGURATION D3, D4) CAUSES AN UP LEVEL AT THE OUTPUTS. A DOWN LEVEL AT THE INPUTS CAUSES A DOWN LEVEL AT THE OUTPUT

2. PIN L IS THE GATE FOR THE LINE DRIVERS. WITH PIN L OPEN CIRCUITED APPROXIMATELY +12V WILL BE PRESENT AND THE LINE DRIVER FUNCTIONS NORMALLY. WITH PIN L GROUNDED THE OUTPUTS (PINS C AND D) REMAIN AT GROUND REGARDLESS OF THE STATE OF THE INPUTS



COMPONENT SIDE

PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
H,G	TLR INPUT		UP	+1.7V	+5.0V
			DOWN	+.7V	0V
A,R	TLR IN PHASE OUTPUT		UP	-0.5V	-0.1V
			DOWN	-5.81V	-8.8V
B,Q	TLR OUT OF PHASE OUTPUT		UP	-0.5V	-0.1V
			DOWN	-5.81V	-8.8V
E,F	TLD INPUT		UP	0.5V	+1.45V
			DOWN	-5.87V	-12.48V
D,C	TLD OUTPUT		UP	+3.11V	+4.09V
			DOWN	+.15V	0V
L	TLD GATE		UP	NOTE 2 (TLD)	
			DOWN	+.35V	-5.8V

DELAYS - NSEC

PIN	DELAY	MIN	MAX
B,Q	TON	67	80
B,Q	TOFF	84	200
A,R	TON	-	234
A,R	TOFF	-	87
	DL		
D,C	TON	-	40
D,C	TOFF	-	225
	GATE		
L	NOT APPLICABLE		

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	STD INTERFACE LINE RECEIVER AND GATED DRIVER				130513					
DESIGN		MODEL	SMS							
DETAIL		SCALE	NONE							
CHECK		DRAW	LIO 5JUL67							
APPRO		CHECK								

2532396

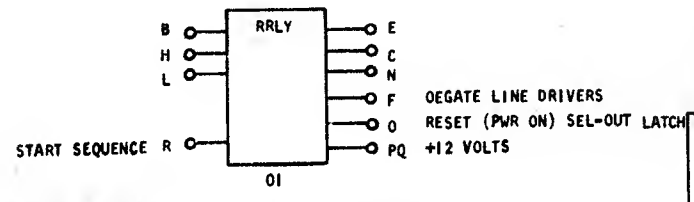
C

2-1

STANDARDS CODE	2532397

CARD CODE	2532397
FRN- P/N 375193	

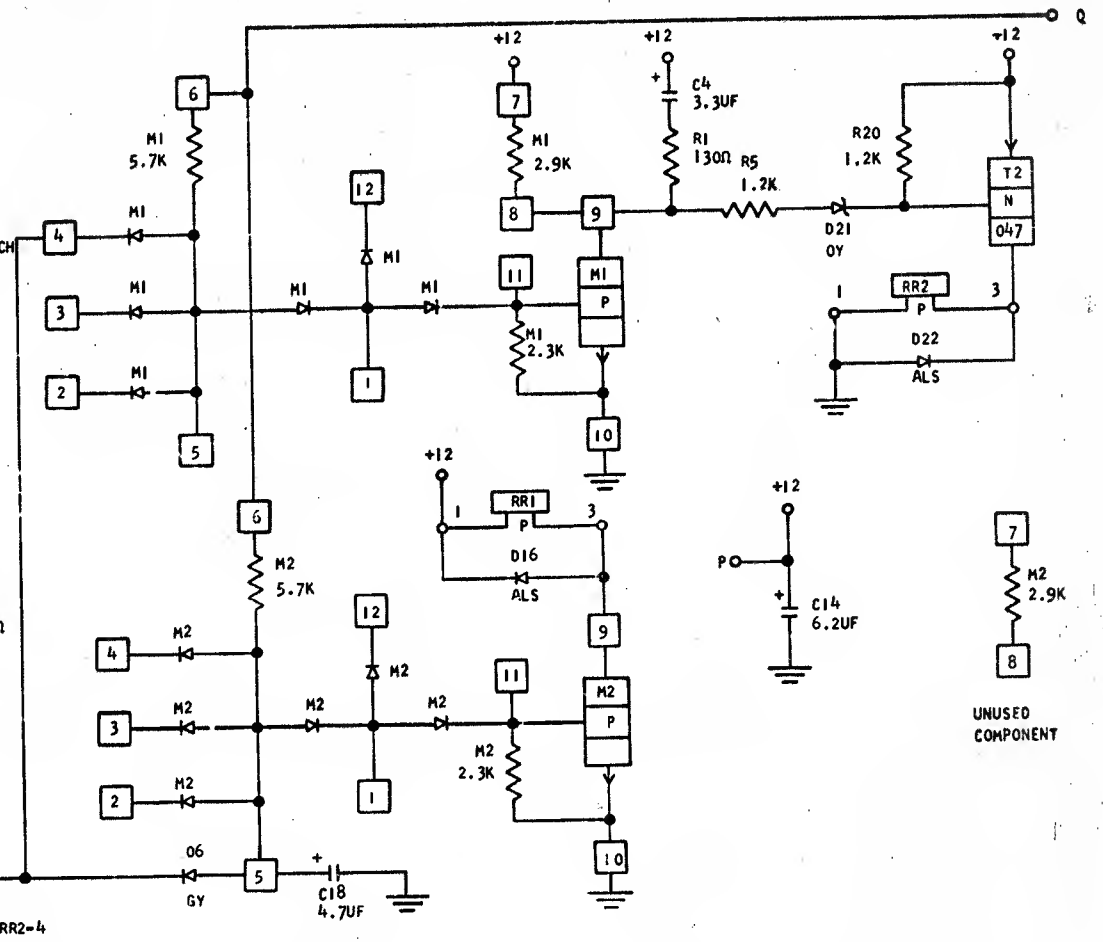
REFERENCE DRAWING
PRODUCTION DRAWING 375193

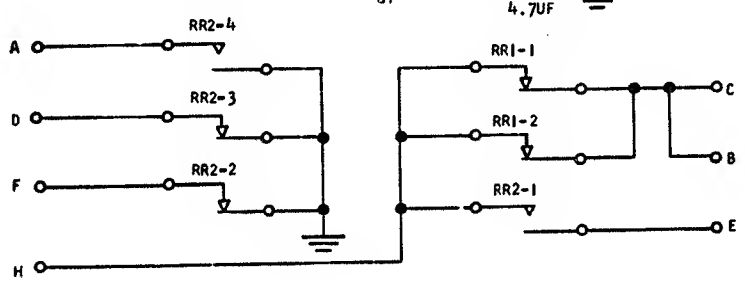


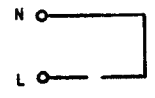
SEQUENCY OF OPERATION

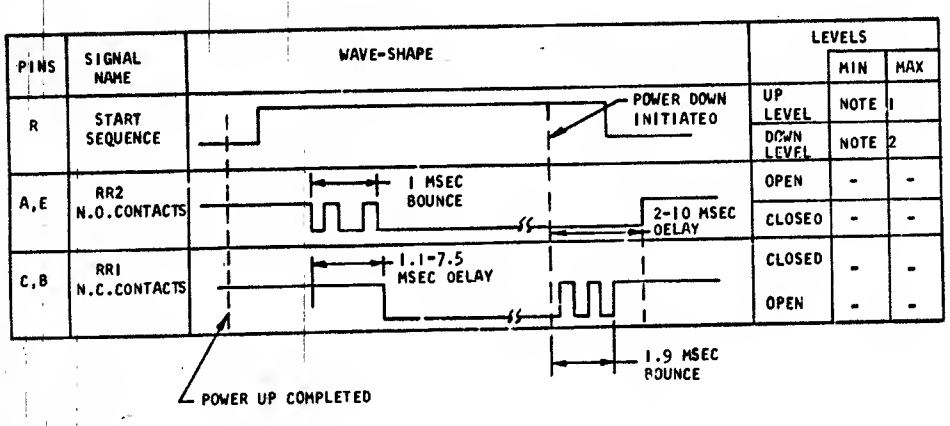
1. IN A POWER-ON SEQUENCE THE CONTACT GROUNO (PIN R) SHOULO NOT BE REMOVEO UNTIL POWER IS UP AND REGULATING. RELAY 2 WILL MAKE 1 MSEC BEFORE RELAY 1.

2. IN A POWER DOWN SEQUENCE RELAY 1 WILL OPOP OUT AT LEAST 2 MSEC OR MORE BEFORE RELAY 2.









COMPONENT SIDE

NOTES:

1. WITH PIN R OPEN THE INPUT CIRCUIT WILL PLACE APPROXIMATELY +12 VOLTS ON PIN R

2. PIN R TIED TO OC GROUND THRU AN EXTERNAL RELAY POINT.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.													
NAME SELECT-OUT SEQUENCE CARD													
DESIGN			MODEL	SMS									
DETAIL			SCALE	NONE									
CHECK			DRAW	LTG 5JUL67									
APPRO			CHECK										

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
	130813					

2532397

C

2-1

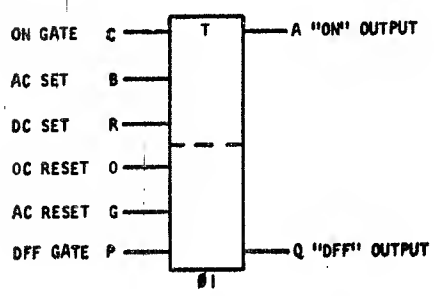
734333

HFT-

P/N: 372575 EC:

REFERENCE DRAWING
PRODUCTION DRAWING 372575

SDTDL HIGH SPEED TRIGGER



OTHER DESIGNATIONS

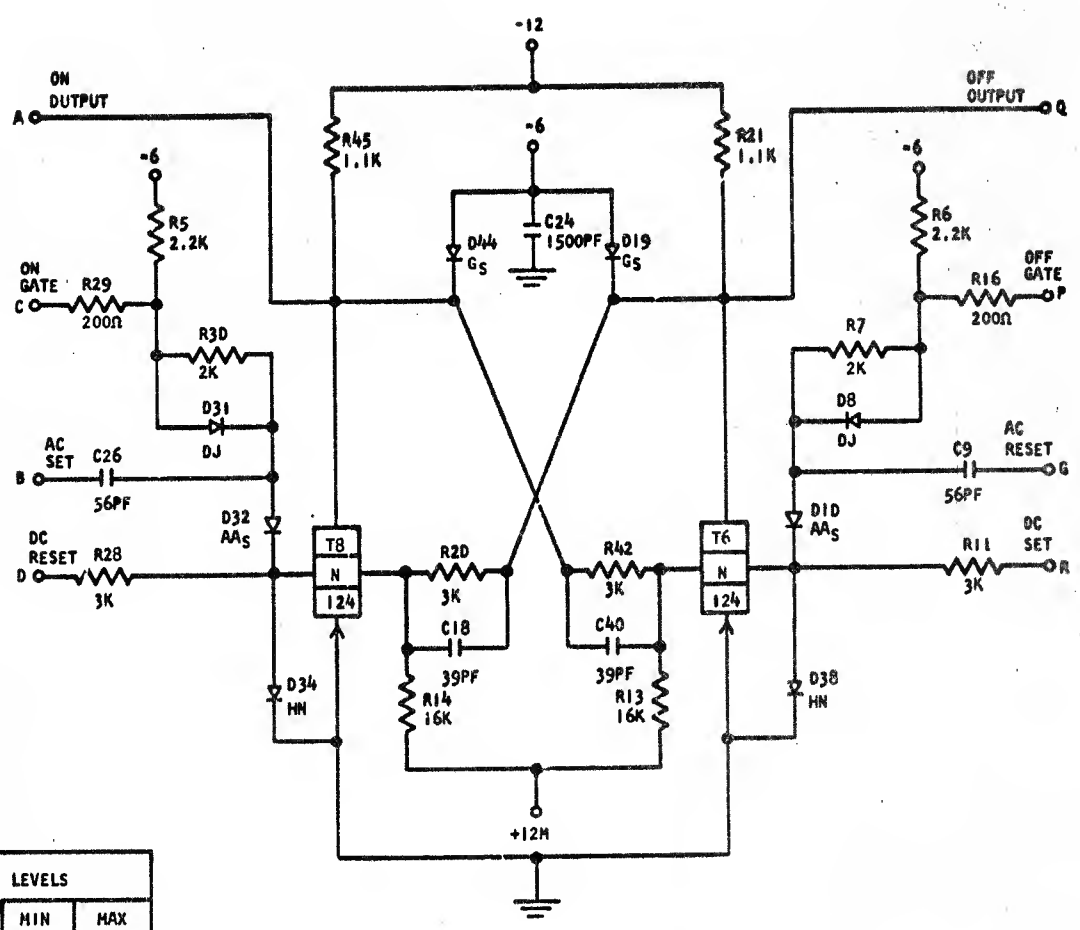
TB

SEQUENCE OF OPERATION

1. WHEN THE TRIGGER IS SET, THE "ON" OUTPUT IS AT -6V ANO THE "OFF" OUTPUT IS OV.
2. WHEN THE TRIGGER IS IN A RESET CONOITION THE "ON" OUTPUT IS AT DV ANO THE "OFF" OUTPUT IS AT -6V.
3. TRIGGER IS SET BY
   (A) A NEGATIVE VOLTACE LEVEL APPLIED TO THE DC SET INPUT OR
   (B) AN UP LEVEL AT THE SET GATE INPUT IN CONJUNCTION WITH A POSITIVE SHIFT AT THE AC SET INPUT.
4. TRIGGER IS RESET BY
   (A) A NEGATIVE VOLTAGE LEVEL AT THE OC RESET INPUT OR
   (B) AN UP LEVEL AT THE RESET GATE INPUT IN CONJUNCTION WITH A PDSITIVE SHIFT AT THE AC RESET INPUT.

NOTES:

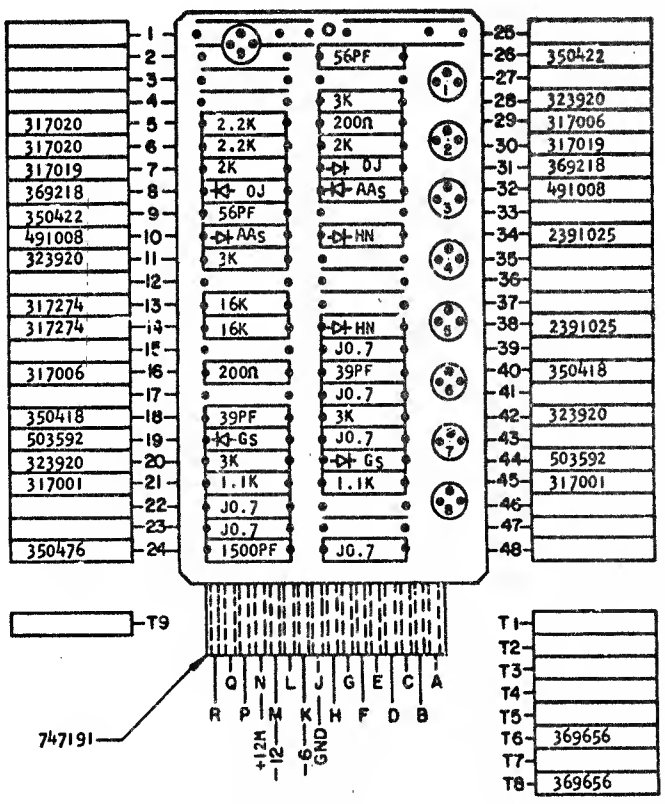
1. THE GATES MUST BE AT THE UP LEVEL 15D NS BEFORE THE AC SET ARRIVES.
2. THE AC SET SHOULD BE AT LEAST 70 NS WIDE AND ITS RISE TIME 70 NS OR LESS.



PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
C	Y	ON GATE		UP	-0.65V	-0.05V
				DOWN	-5.81V	-7.64V
B	Y	AC SET		UP	-0.65V	-0.05V
				OOWN	-5.81V	-7.64V
G	Y	AC RESET		UP	-0.65V	-0.05V
				DOWN	-5.81V	-7.64V
P	Y	DFF GATE		UP	-0.65V	-0.05V
				OOWN	-5.81V	-7.64V
R	Y	DC SET		Uf	-D.65V	-0.05V
				OOWN	-5.81V	-7.64V
D	Y	OC RESET		UP	-0.65V	-0.05V
				OOWN	-5.81V	-7.64V
A	Y	"ON" OUTPUT		UP	-0.65V	-0.05V
				DOWN	-6.26V	-7.64V
Q	Y	"OFF" OUTPUT		UP	-0.65V	-0.05V
				DOWN	-6.26V	-7.64V

DELAY - NSEC

	TON MAX	TON MIN	TRISE MAX	TRISE MIN	TDFF MAX	TDFF MIN	TFALL MAX	TFALL MIN
BINARY OPERATIDN:	133	36	63	16	240	115	200	95
GATED:	135	4D	60	16	255	82	21D	61



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.														
NAME	SDTDL HIGH SPEED TRIGGER													
DESIGN			MODEL	SMS 1440										
DETAIL			SCALE	NONE										
CHECK			DRAW	MDE 4-16-63										
APPRO	KES 4-24-63		CHECK											

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
4-24-63	116800c					
4-29-65	124282	GLK				
9AUG66	127574	GLK				

734333

C

24

734417

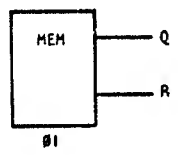
734417

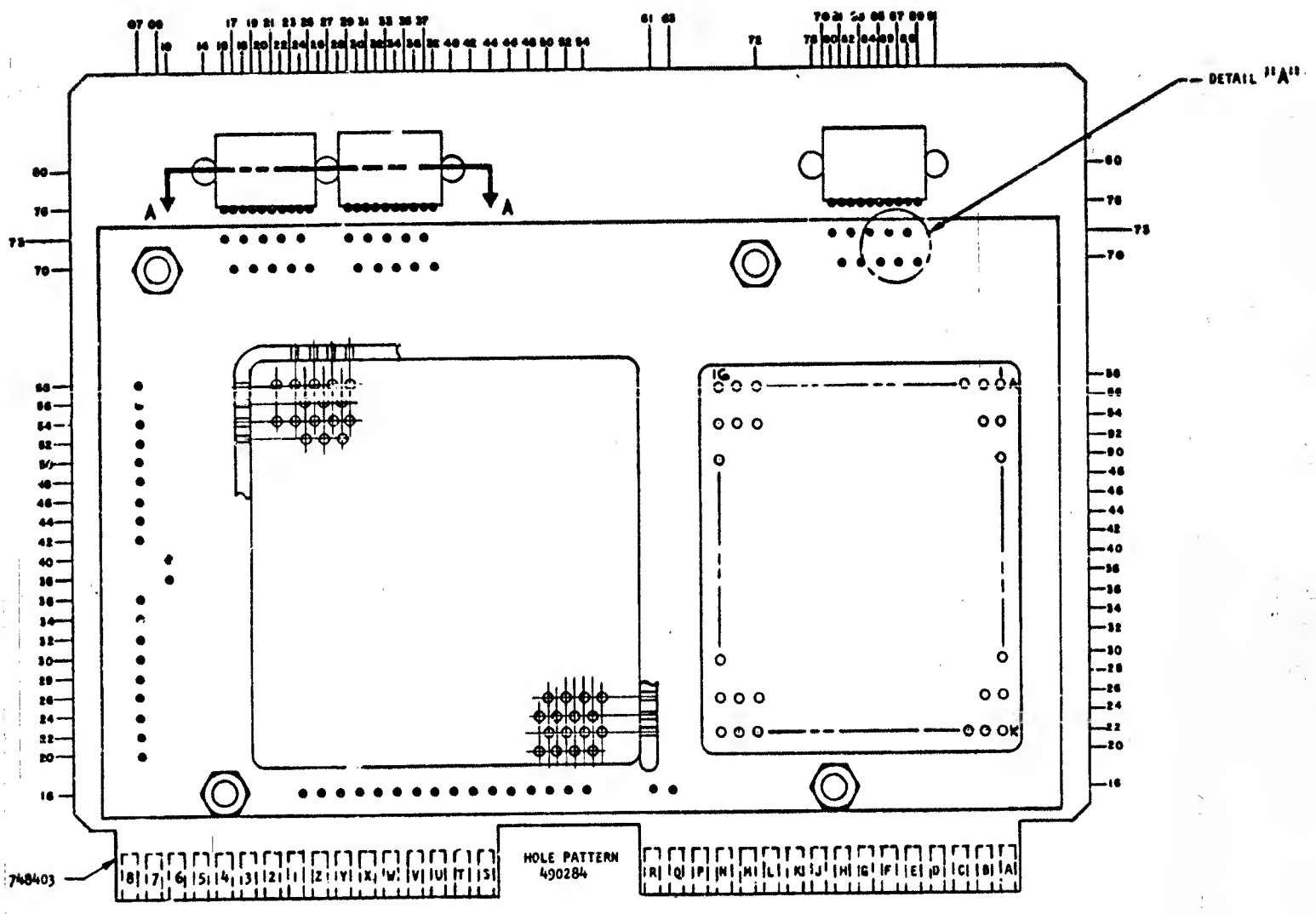
HGA-

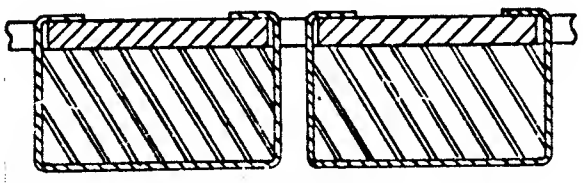
P/N: 373373 EC: 0117834

REFERENCE DRAWING
PRODUCTION DRAWING 373373

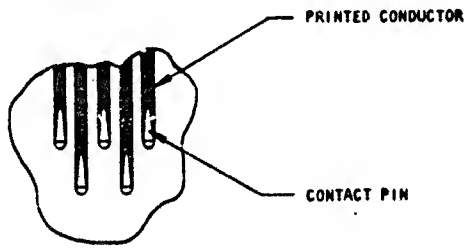
ROW BIT







SECTION A-A
SCALE 4/1



DETAIL "A"

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME ROW BIT					9-16-63	116800F					
DESIGN		MODEL	SMS 1460								
DETAIL		SCALE	NONE								
CHECK		DRAW	LIG 9-4-63								
APPRO		CHECK									

734417

C

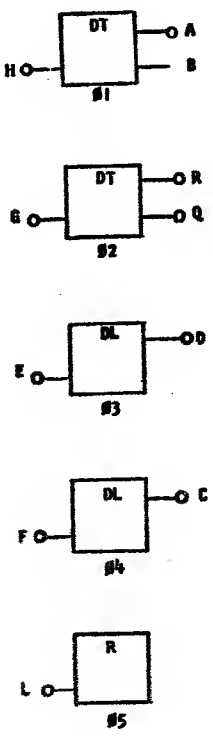
STANDARDS CODE 846924

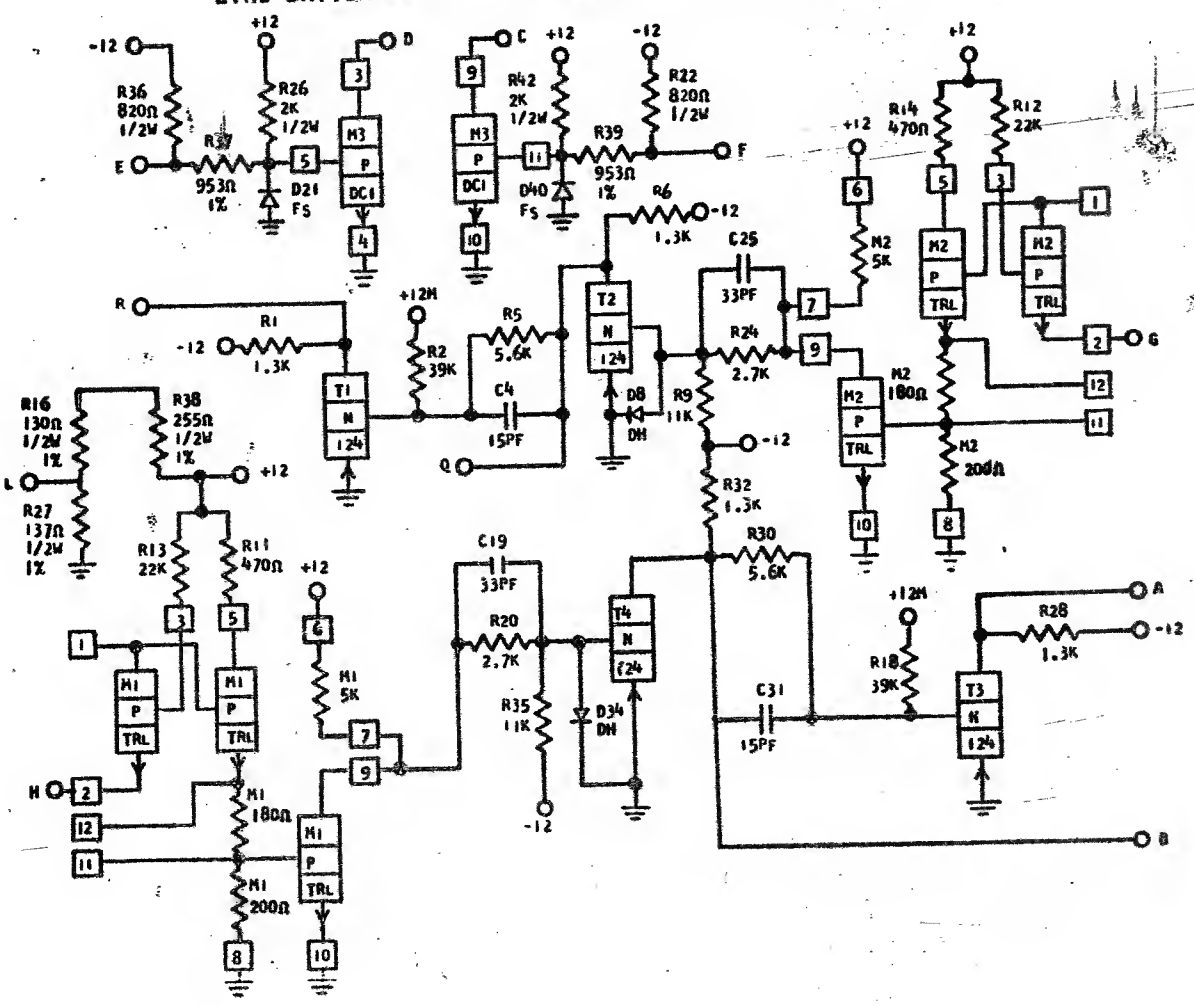
REFERENCE DRAWING
PRODUCTION DRAWING 374791

CARD CODE 846924

JEA-
P/N 374791

LINE DRIVER AND RECEIVER NAND TO SLT-SLT TO NAND





NOTES:

1. THE TRANSMISSION LINE DRIVES, DL, CONVERT FROM SDTDL LEVELS TO SLT STANDARD INTERFACE LEVELS.
2. THE TRANSMISSION LINE RECEIVERS,DT, CONVERT FROM SLT STANDARD INTERFACE LEVELS TO SDTDL LEVELS.
3. THE RESISTOR NETWORK, R, IS USED TO TERMINATE THE SLT STANDARD INTERFACE.

SEQUENCE OF OPERATION

TRANSMISSION LINE RECEIVER:

1. AN UP LEVEL AT THE INPUT TO THE DT CAUSES AN UP LEVEL AT PINS B, Q AND AN OUT OF PHASE DOWN LEVEL AT PINS A, R. A DOWN LEVEL AT THE INPUT CAUSES PINS B, Q TO GO TO A DOWN LEVEL AND PINS A, R TO AN UP LEVEL.

TRANSMISSION LINE DRIVER:

1. AN UP LEVEL INPUT CAUSES A DOWN LEVEL AT THE OUTPUT. A DOWN LEVEL INPUT CAUSES AN UP LEVEL AT THE OUTPUT.

PINS		SIGNAL NAME	WAVESHAPE		LEVELS MIN	LEVELS MAX
H,G		TLR INPUT		UP	+2.1V	+3.4V
				DOWN	+1.20V	+0.14V
B,Q	Y	TLR IN PHASE OUTPUT		UP	-0.5V	-0.1V
				DOWN	-5.81V	-8.8V
A,R	Y	TLR OUT OF PHASE OUTPUT		UP	-0.5V	-0.1V
				DOWN	-5.81V	-8.8V
E,F	Y	TLD INPUT		UP	-0.53V	+1.45V
				DOWN	-5.87V	-10.5V
D,C		TLD OUTPUT		UP	+2.1V	+3.4V
				DOWN	+0.33V	0.00V
L		LINE TERMINATOR		UP	+2.1V	+3.4V
				DOWN	+1.26V	+0.14V

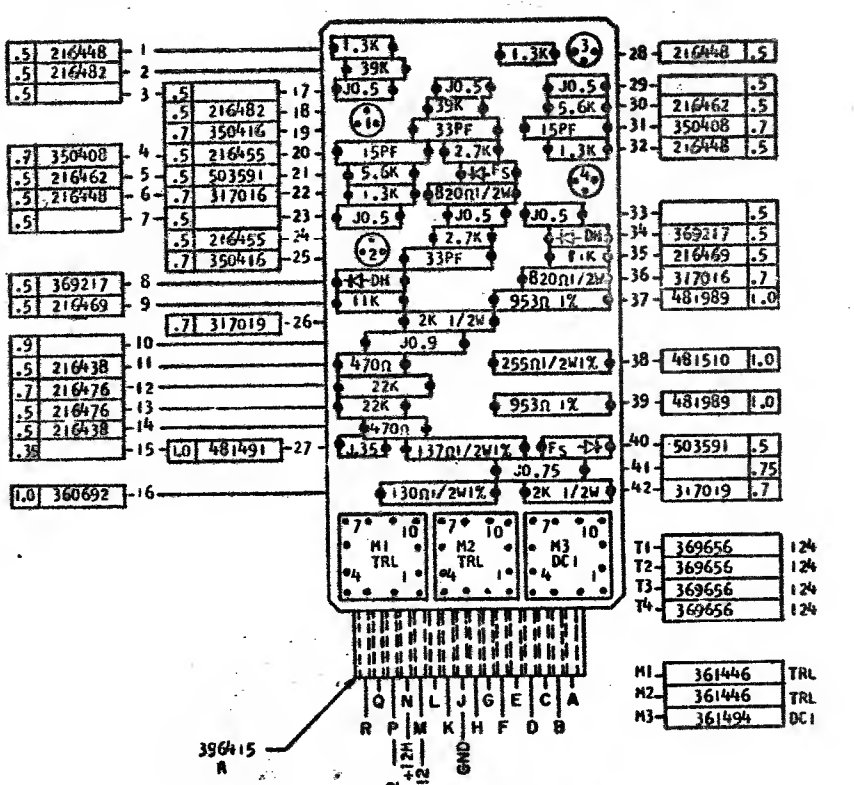
DELAY - NSEC

DT

PIN	DELAY	MIN	MAX
B,Q	T_{ON}	20	120
B,Q	T_{OFF}	60	340
A,R	T_{ON}	120	390
A,R	T_{OFF}	28	138

DL

D,C	T_{ON}	15	215
D,C	T_{OFF}	100	700



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	LINE DRIVER AND RECEIVER - NAND TO SLT - SLT TO NAND				16DEC65	125840	4ZX				
DESIGN			MODEL	SMS		125840					
DETAIL			SCALE	NONE							
CHECK			DRAW	JD 3DEC65							
APPRO			CHECK	JD 6DEC65							

846924

C

374792

VOLTAGE SEQUENCING CARD

374792 JEB-

STANDARDS CODE 2-7045

-20 R8 750Ω — RR1 (3 P 1) — D21 ALS — T1 (P 083)

R7 680Ω

-20 R5 1.58K 1% — RR2 (3 P 1) — +12 — D24 ALS — T4 (P 083)

R3 750Ω 1% — C18 22UF — D25 DK

-12 SENSE INPUT

+12 SENSE INPUT — +12 R16 430Ω 2W

-12 R9 560Ω — T2 (P 083) — R10 360Ω

G R19 330Ω — T3 (P 083) — R2 470Ω — HEATSINK — RR3 (3 P 1) — D13 ALS

-6 SENSE INPUT — C11 22UF

RR1-2 — RR2-1 — F

D

-20V — RR1-1 — RR2-2 — RR3-1 — A

C C29 .051UF

B C30 .051UF

E C28 .051UF

1	0.6		
2	0.7	317011	
3	1.0	481548	
4	0.5		
5	1.0	481575	
6	0.4		
7	0.7	317014	
8	0.7	317015	
9	0.7	322347	
10	0.7	528937	
11	1.0	222093	
12	0.5		
13	0.5	2106333	
14	0.4		
15	0.5		
16	1.0	492644	
17	0.3		
18	1.0	222093	
19	0.7	317428	
20	0.3		

ALS-D — J0.6 — LOC HOLE 1-2, 1-1 RR1 — 470Ω — 750Ω 1% — J0.4 — J0.5 — J0.3 — 1.58K 1% — ALS — J0.4 — 680Ω — 750Ω — 560Ω — RR2 LOC HOLE 2-1, 2-2 — 360Ω — DK — 22UF + — J0.3 — J0.5 — J0.65 — ALS-D — LOC HOLE 3-1 RR3 — J0.4 — J0.5 — .051UF — 430Ω 2W — J0.3 J0.3 — .051UF — + 22UF — 330Ω — .051UF

21	2106333	0.5	
	766043		
	483316		(8)
22		0.4	
23		0.3	
24	2106333	0.5	
	766043		
	483316		(8)
25	369216	0.5	
26		0.3	
27		0.65	
	766040		
	483316		(6)
28	217054	1.0	
29	217054	1.0	
30	217054	1.0	

T1	318325	083
T2	318325	083
**T3	318325	083
T4	318325	083

R P M K GND — -20 +12 -12 -6

396417

COMPONENT SIDE

HOLE PATTERN 396471

NOTES

X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 893667

XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396, 891999 AND 892058

XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED

XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296

** XIV ASSEMBLE TRANSISTOR T3 WITH HEATSINK PART NUMBER 492434 OR 492435

XV REED RELAYS PART NUMBERS 766040 AND 766043 MUST NOT BE SUBJECTED TO LIQUIDS

* XVI SLOT IN LUG 483316 MUST BE MOUNTED PARALLEL TO Y-Y AXIS

B FW 28NOV67

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
WRW	8-26-64

INTERNATIONAL BUSINESS MACHINES CORP.													
NAME	CARD ASM TSTR- VOLTAGE SEQUENCING CARD						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
DESIGN			MODEL				10-23-64	122677	GLK				~~X1635B~~
DETAIL			SCALE	NONE			5DEC67	132379	GWS				
CHECK	DCH	10-19-64	DRAW	LIG	7-24-64								CIRCUIT FAMILY
APPRO	GLK	10-19-64	CHECK										NAND

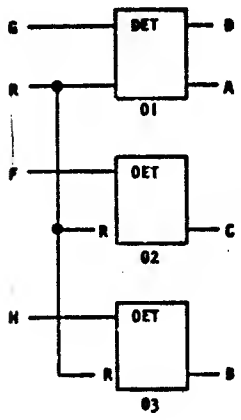
374792

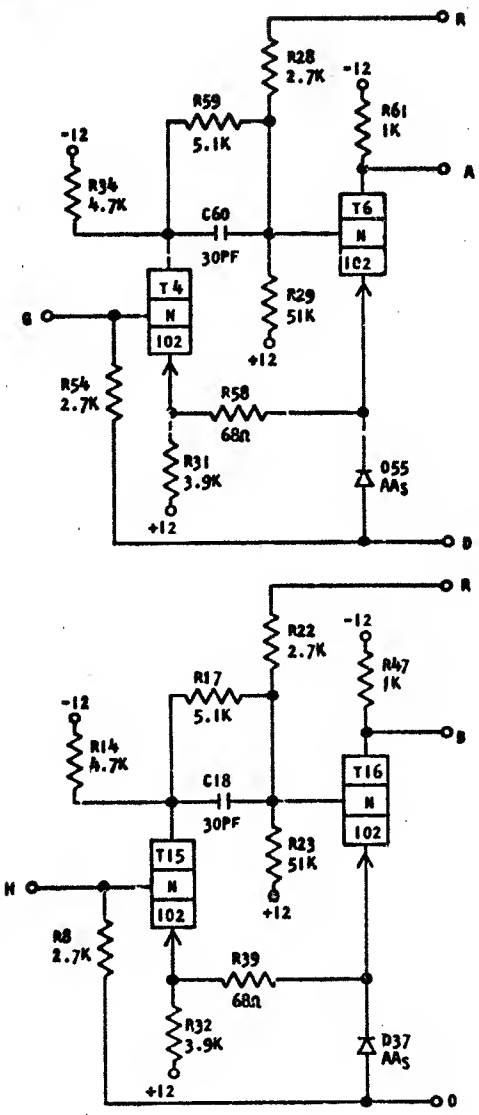
STANDARDS CODE	
743068	

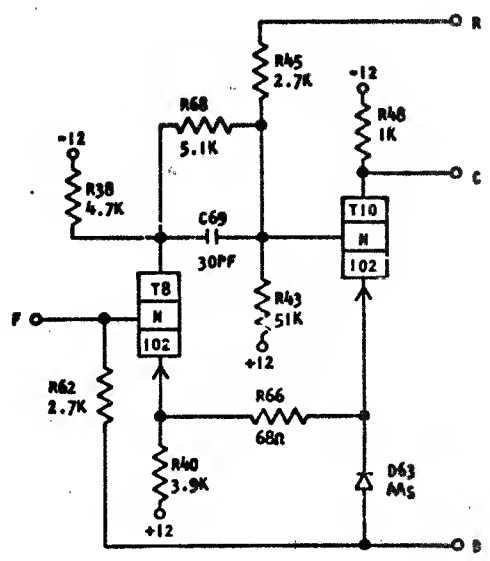
CARD CODE	743068
UGR-	

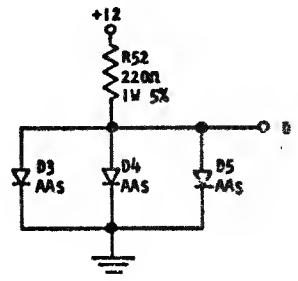
REFERENCE DRAWING
PRODUCTION DRAWING 372992
EC:120691

SENSE AMP DETECTOR









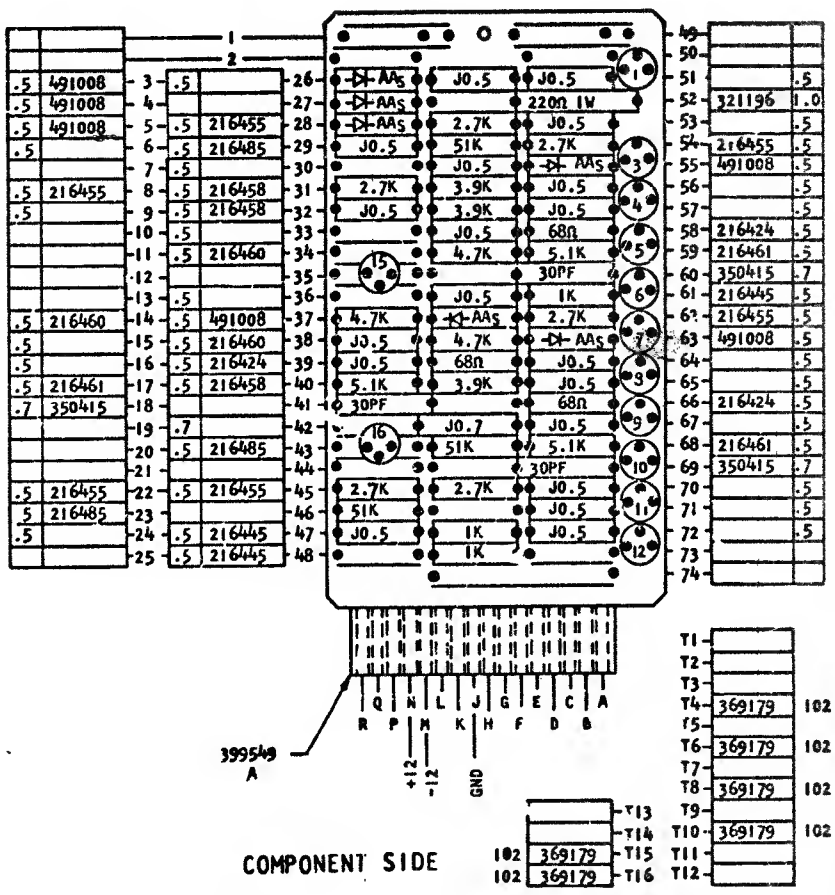
SEQUENCE OF OPERATION

1. .WHEN INPUT PIN G GOES DOWN, T4 TURNS ON, T6 TURNS OFF AND THE OUTPUT GOES DOWN.

NOTE:
INPUT PIN R MUST BE AT THE UP LEVEL WHEN THE INPUT PIN G GOES DOWN.

PINS	SIGNAL NAME	WAVESHAPE READ / WRITE	LEVELS	MIN	MAX
G	INPUT			.5V	1.5V
R	STROBE INPUT		UP	+0.27V	+0.57V
			DOWN	-9.3V	-13.5V
A	OUTPUT		UP	-.970V	-.469V
			DOWN	DEPENDENT ON LOAD	

DELAY	MIN	MAX
T_{ON} (NSEC)	35	76
T_{OFF} (NSEC)	43	180



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.														
NAME	SEMSE AMP DETECTOR													
DESIGN			MODEL	SMS 1440										
DETAIL			SCALE	NONE										
CHECK			DRAW	LIG	10NOV67									
APPRO	GWS	8APR64	CHECK											

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
8APR64	121005	GWS				743068
12NOV64	122706	GLK				
16NOV67	132328					

C

GILVIE PRESS, INC., BROOKLYN 17, N. Y. STOCK NO. 6007

SHEET OF EC.

2-1

822929

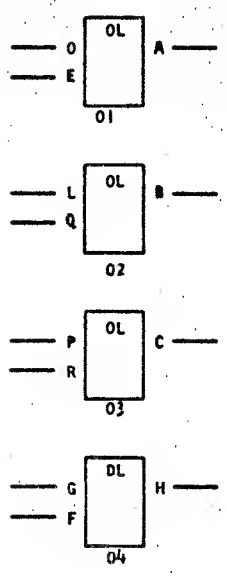
STANDARDS CODE
2-7045

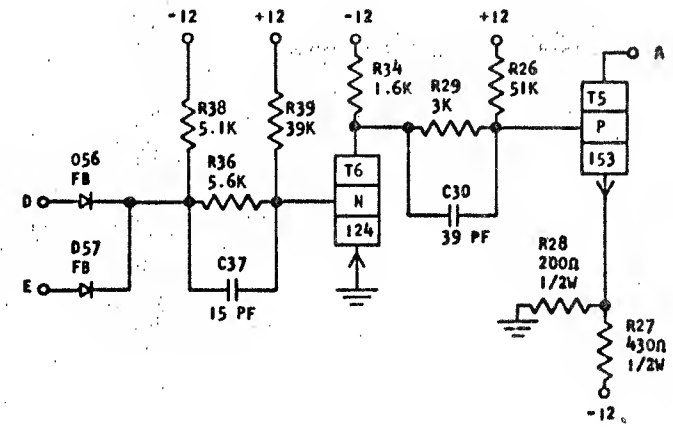
822929

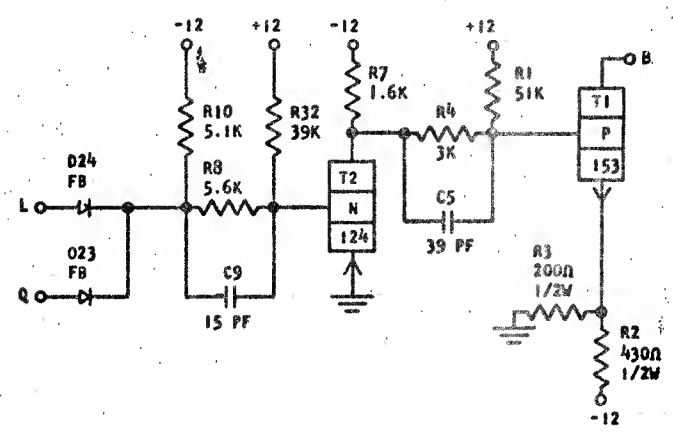
UGT-

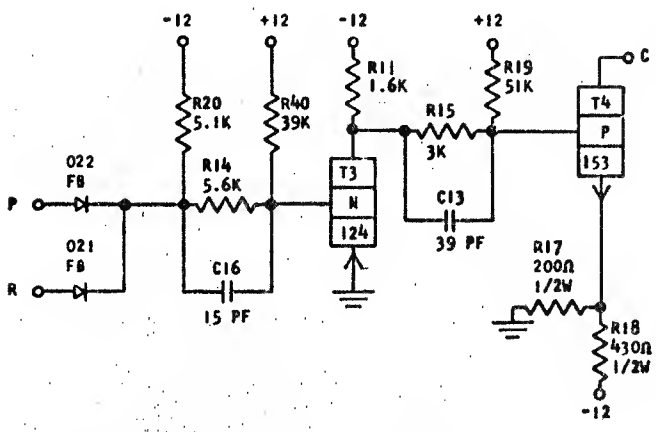
822929

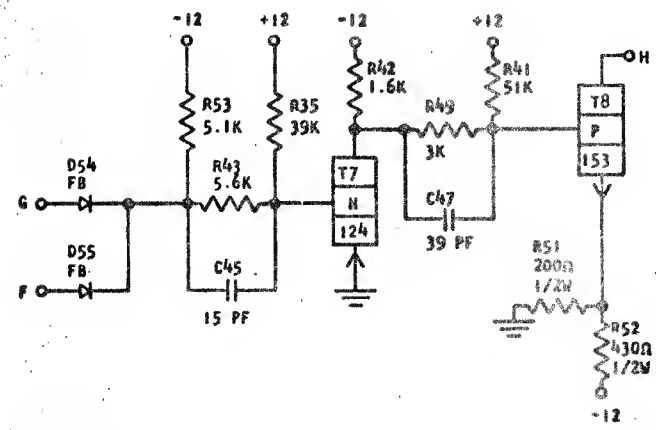
REFERENCE DRAWING
SEE PRODUCTION DRAWING 372976











CIRCUIT OPERATION

1. EITHER INPUT UP, OUTPUT TRANSISTOR OFF, OUTPUT UP.
2. BOTH INPUTS DOWN, OUTPUT TRANSISTOR ON, OUTPUT DOWN.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN.	LEVELS MAX.
O,L P,G	Y	INPUT		UP	-0.65V	-0.05V
				DOWN	-5.81V	-12.48V
E,Q R,F	Y	INPUT		UP	-0.65V	-0.05V
				DOWN	-5.81V	-12.48V
A,B C,H		OUTPUT		UP	OUTPUT OPEN CIRCUIT LEVEL DEPENDS ON TERM.	
				DOWN	-1.25V	-1.76V

DELAY - NS

TURN ON DELAY

WITH SDTDL OR SDTRL RECEIVER

120 + C

WITH CTDL RECEIVER

380 + C

TURN OFF DELAY

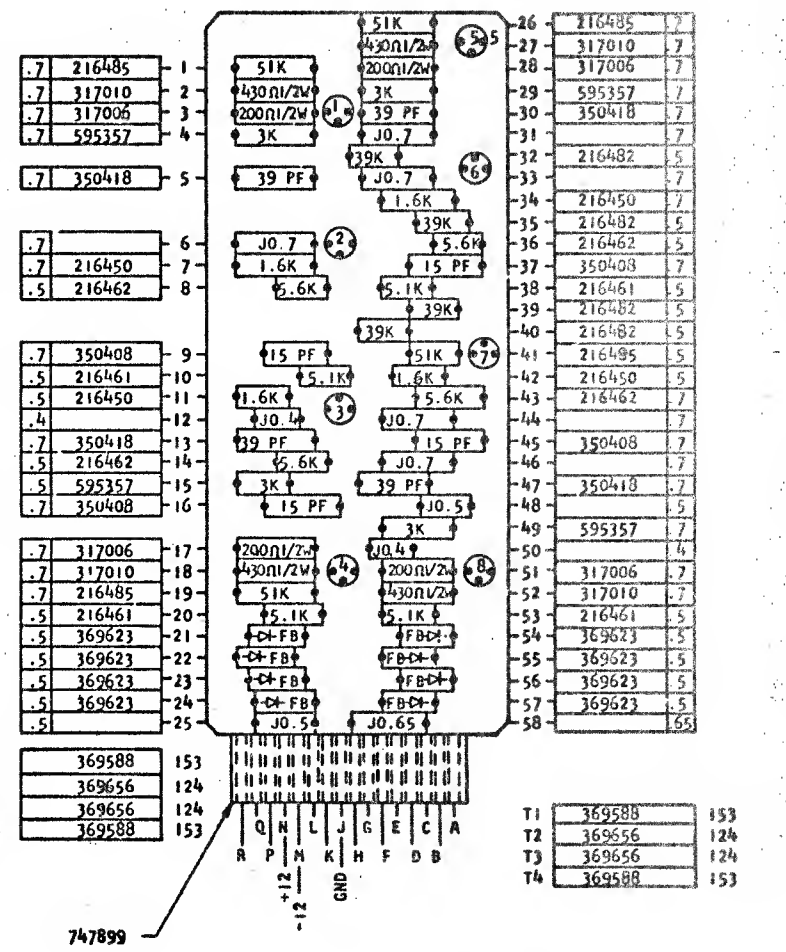
SDTDL OR SDTRL RECEIVER
110 + C

CTDL RECEIVER
200 + C

WHERE C = DELAY INTRODUCED BY CABLE, ADD 2 NS PER FOOT OF CABLE.

NOTE: DELAYS MEASURED FROM INPUT OF DRIVER TO OUTPUT OF TERMINATING CIRCUIT.

C



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	23APR64

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASH TSTR-NON INVERTING SIMPLEX INTERFACE LINE DRIVER				
DESIGN			MODEL	SMS-1444	
DETAIL			SCALE	NONE	
CHECK			DRAW	VMD	17FEB66
APPRD			CHECK		

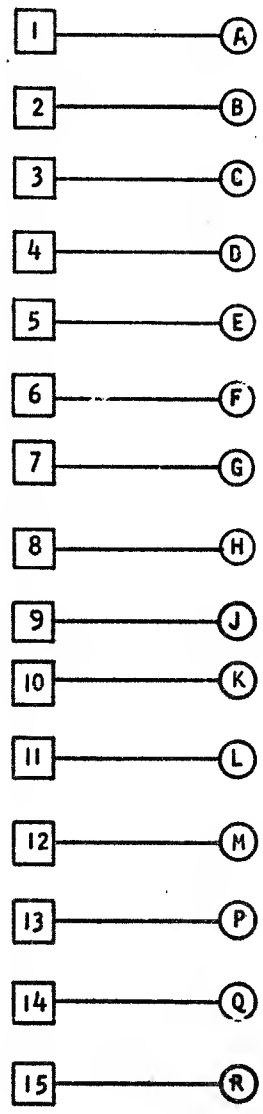
DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
2JUN64	121287					
1MAR66	126404					
						CIRCUIT FAMILY SDTDL

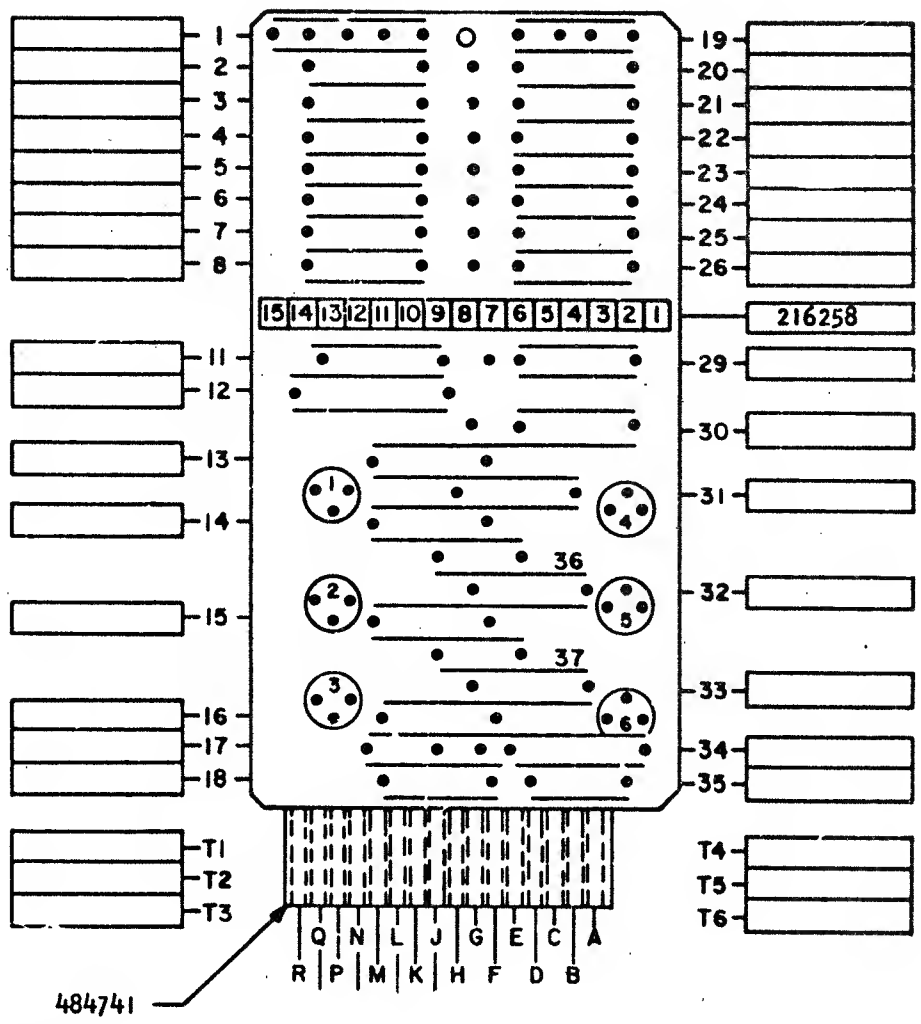
476778

JUMPER CARD

370858

370858	Y3 --
STANDARDS CODE	2-7045





NOTES

X ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999

XI REFERENCE 216259 MALE CONTACT STRIP TO BE USED AS REQUIRED

B

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
KMT	11-6-61

HOLE PATTERN 491020

COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	370858
NAME	CARD ASM TSTR - JUMPER CARD					11-29-61	113105	DWB				2547-1718	
						8-6-62	D114709	MDL					
DESIGN	JPC	10-24-61	MODEL	SMS 7909									
DETAIL	JPC	10-24-61	SCALE	NONE									
CHECK	HRT	11-17-61	DRAW	VE	11-10-61								
APPRO	GWS	11-29-61	CHECK	JDJ	11-15-61								

82-3974-1* 6-22-61

2-1

734392

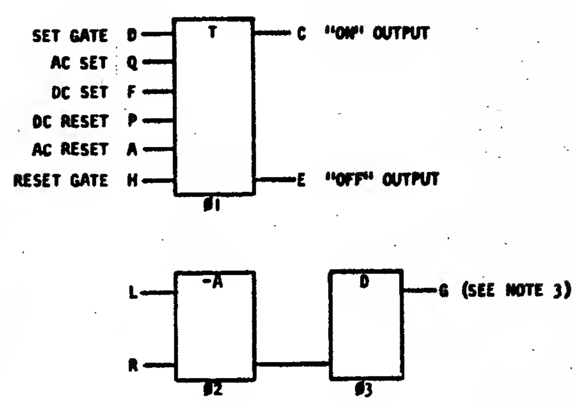
YKR-

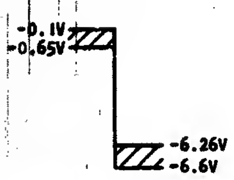
P/N: 372220 EC:

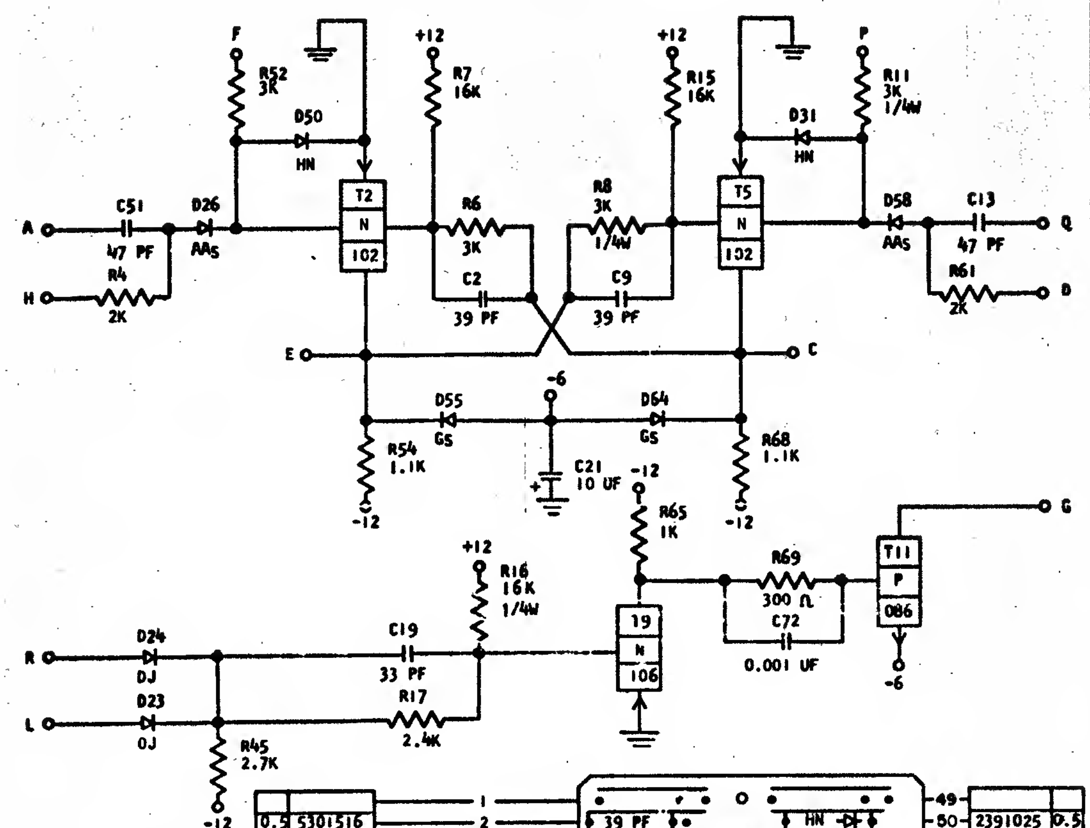
734392

REFERENCE DRAWING
PRODUCTION DRAWING 372220

DATA REGISTER AND INHIBIT DRIVER







OTHER DESIGNATIONS
CONF. 2 +0
CONF. 3 DR

SEQUENCE OF OPERATION

FOR TRIGGER

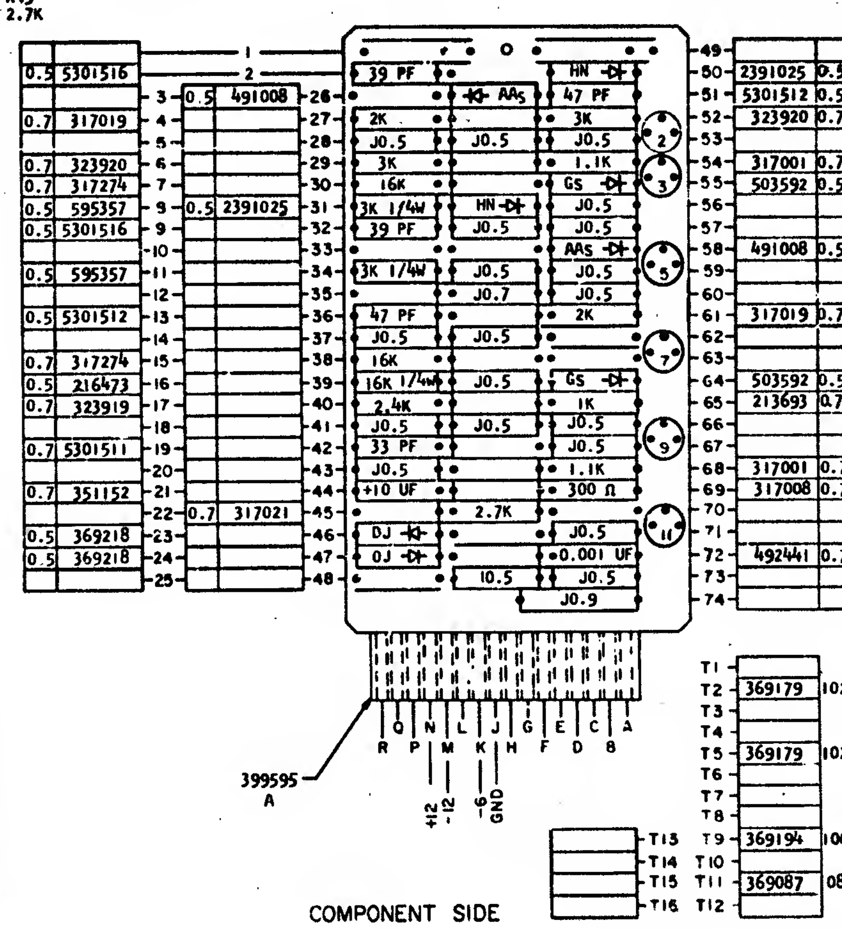
1. WHEN THE TRIGGER IS SET, THE "ON" OUTPUT IS AT -6V AND THE "OFF" OUTPUT IS 0V.
2. WHEN THE TRIGGER IS IN A RESET CONDITION THE "ON" OUTPUT IS AT 0V AND THE "OFF" OUTPUT IS AT -6V.
3. TRIGGER IS SET BY
   A) A NEGATIVE VOLTAGE LEVEL APPLIED TO THE DC SET INPUT OR
   B) AN UP LEVEL AT THE SET GATE INPUT IN CONJUNCTION WITH A POSITIVE SHIFT AT THE AC SET INPUT.
4. TRIGGER IS RESET BY
   A) A NEGATIVE VOLTAGE LEVEL AT THE DC RESET INPUT OR
   B) AN UP LEVEL AT THE RESET GATE INPUT IN CONJUNCTION WITH A POSITIVE SHIFT AT THE AC RESET INPUT.

FOR INHIBIT DRIVER

1. PINS L AND R DOWN WILL TURN THE DRIVER ON.
2. PIN L OR R UP WILL TURN THE DRIVER OFF.

NOTES

1. THE GATES MUST BE AT THE UP LEVEL 150NS BEFORE THE AC SET ARRIVES.
2. THE AC SET SHOULD BE AT LEAST 70NS WIDE AND ITS RISE TIME 70NS OR LESS.
3. NO OUTPUT VOLTAGE IS SPECIFIED SINCE THE CIRCUIT IS A CURRENT DRIVER.



COMPONENT SIDE

PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
D	V	SET GATE		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
Q	V	AC SET		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
A	V	AC RESET		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
H	V	RESET GATE		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
F	V	DC SET		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
P	V	DC RESET		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
C	V	"ON" OUTPUT		UP	-.65V	-.1V
				DOWN	-6.26V	-7.64V
E	V	"OFF" OUTPUT		UP	-.65V	-.1V
				DOWN	-6.26V	-7.64V

DELAY (NSEC)

TRIGGER

	T_{ON} MAX	T_{ON} MIN	T_{RISE} MAX	T_{RISE} MIN	T_{OFF} MAX	T_{OFF} MIN	T_{FALL} MAX	T_{FALL} MIN
BINARY OPERATION:	133	36	63	16	240	115	200	95
GATED:	135	40	48	16	205	82	160	61

INHIBIT DRIVER

	MAX	MIN
T_{ON}	350	100
T_{OFF}	625	625

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	DATA REGISTER AND INHIBIT DRIVER			4-17-63	116800A					734392
DESIGN		MODEL	SMS 1440	9-15-64	121632					
DETAIL		SCALE	NONE	3-12-65	123723					
CHECK		DRAW	MOE 2-20-63							
APPRO	4-17-63	CHECK								

C

734393

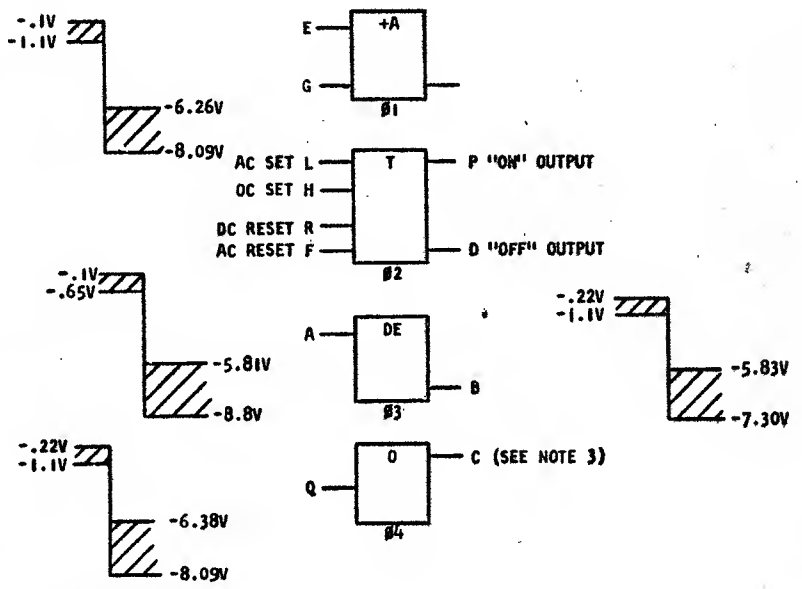
YKS—

P/N: 372221

734393

REFERENCE DRAWING
PRODUCTION DRAWING 372221

SDTDL - ADDRESS REGISTER



OTHER DESIGNATIONS

CONF. 1	-0
CONF. 4	DR

SEQUENCE OF OPERATION

FOR TRIGGER

1. WHEN THE TRIGGER IS SET, THE "ON" OUTPUT IS AT -6V AND THE "OFF" OUTPUT IS OV.
2. WHEN THE TRIGGER IS IN A RESET CONDITION THE "ON" OUTPUT IS AT OV AND THE OFF OUTPUT IS AT -6V.
3. TRIGGER IS SET BY
   A) A NEGATIVE VOLTAGE LEVEL APPLIED TO THE DC SET INPUT OR
   B) PINS E AND G UP WHICH RESULTS IN AN UP LEVEL AT THE SET GATE INPUT IN CONJUNCTION WITH A POSITIVE SHIFT AT THE AC SET INPUT.
4. TRIGGER IS RESET BY A NEGATIVE VOLTAGE LEVEL AT THE DC RESET INPUT.

FOR NON-INVERTING POWER DRIVER

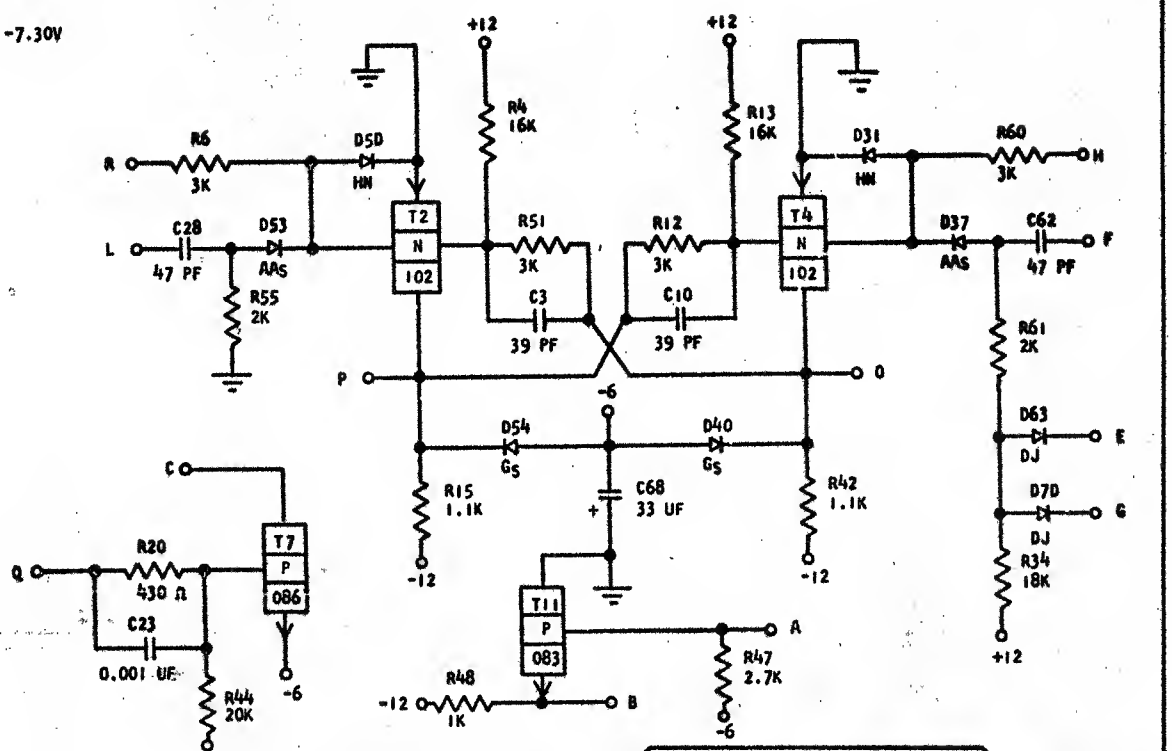
1. INPUT UP: TRANSISTOR (T11) ON, OUTPUT UP
2. INPUT OOWN: TRANSISTOR (T11) OFF, OUTPUT DOWN

FOR BIAS DRIVER

1. INPUT UP: TRANSISTOR (T7) ON; INPUT DOWN: TRANSISTOR (T7) OFF.

NOTES

1. GATE INPUTS E AND G MUST BE AT THE UP LEVEL 15ONS BEFORE THE AC SET ARRIVES.
2. THE AC SET SHOULD BE AT LEAST 70NS WIDE AND ITS RISE TIME 70NS OR LESS.
3. NO OUTPUT VOLTAGE IS SPECIFIED SINCE THE CIRCUIT IS A CURRENT DRIVER.



PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
L	Y	AC SET		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
F	Y	AC RESET		UP	-.65V	-.1V
				OOWN	-5.81V	-7.64V
H	Y	DC SET		UP	-.65V	-.1V
				OOWN	-5.81V	-7.64V
R	Y	DC RESET		UP	-.65V	-.1V
				DOWN	-5.81V	-7.64V
P	Y	"ON" OUTPUT		UP	-.65V	-.1V
				DOWN	-6.26V	-7.64V
D	Y	"OFF" OUTPUT		UP	-.65V	-.1V
				DOWN	-6.26V	-7.64V

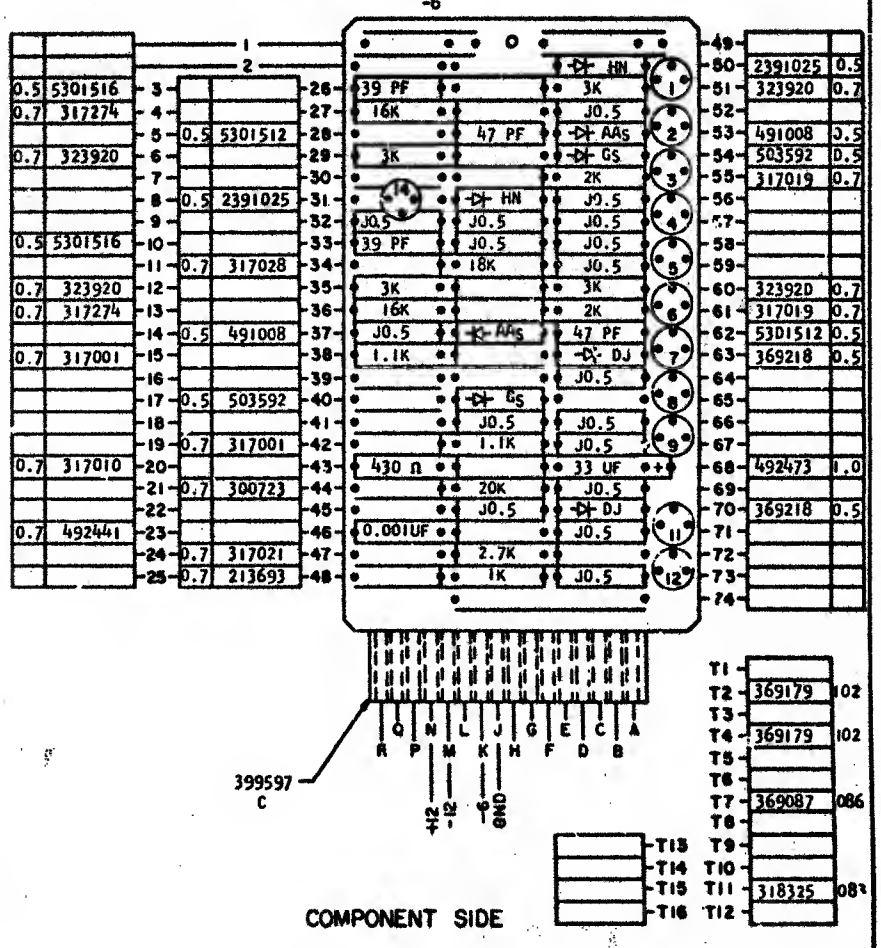
DELAY - NSEC

TRIGGER

	T_{ON} MAX	T_{ON} MIN	T_{RISE} MAX	T_{RISE} MIN	T_{OFF} MAX	T_{OFF} MIN	T_{FALL} MAX	T_{FALL} MIN
BINARY OPERATION:	133	36	63	16	240	115	200	95
GATED:	135	40	48	16	205	82	160	61

NON-INVERTING POWER DRIVER

	MAX	MIN
T_{ON}	20	6
T_{OFF}	28	6



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	SDTDL - ADDRESS REGISTER				
DESIGN			MODEL	SMS 1440	
DETAIL			SCALE	NONE	
CHECK			DRAW	MDE	2-21-63
APPRO		3-25-63	CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
3-25-63	116800					
4-23-64	120090	GWS				
9-15-64	121632					
9AUG66	127574	GLK				

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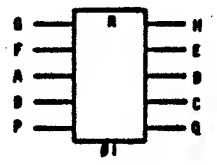
P/N: 372222 EC: 0114425

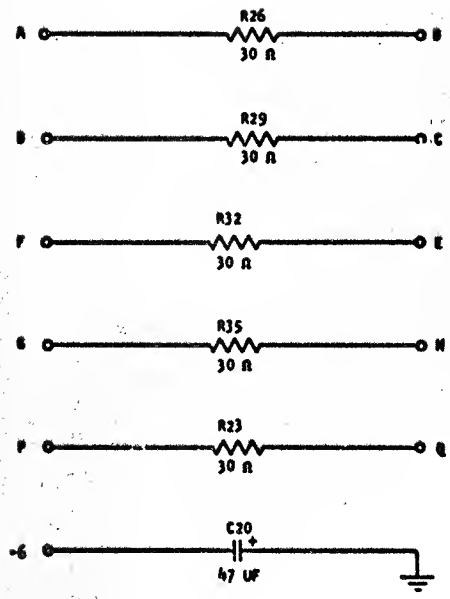
REFERENCE DRAWING
PRODUCTION DRAWING 372222

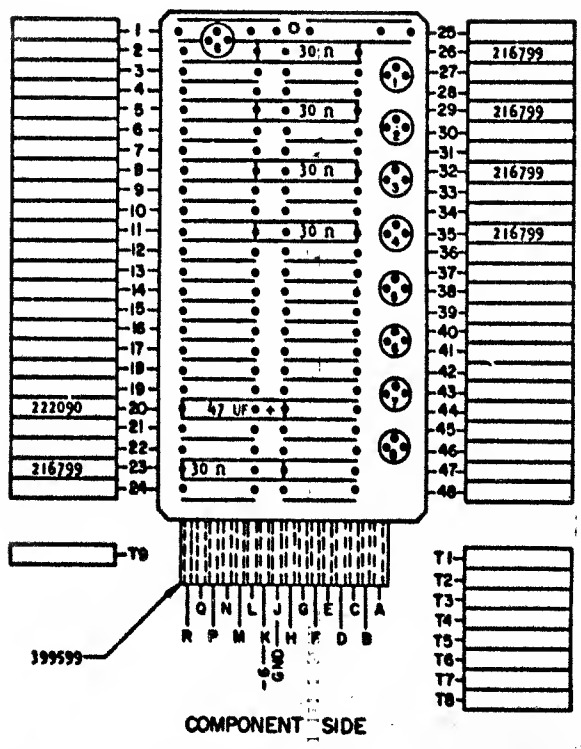
BIAS LOAD



APPLICATION

USED TO DETERMINE THE AMOUNT OF BIAS CURRENT DRAWN FROM THE BIAS DRIVER THROUGH THE SWITCH CORES.





INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	BIAS LOAD					3-20-63	116800					
DESIGN			MODEL	SMS 1440								
DETAIL			SCALE	NONE								
CHECA			DRAW	MOE	2-20-63							
APPRO	RES	3-25-63	CHECA									

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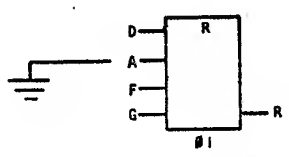
P/N: 372223 EC: 0114426

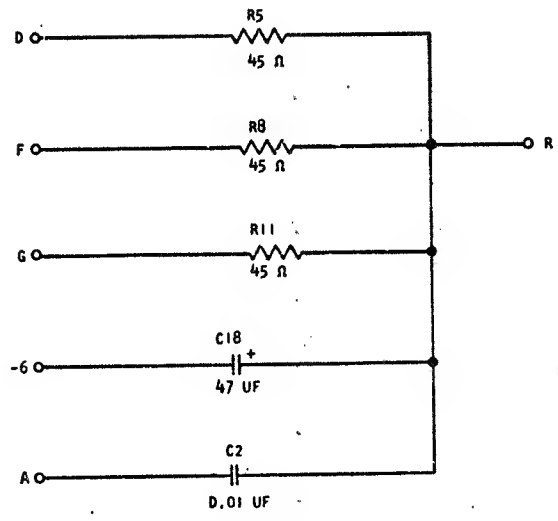
REFERENCE DRAWING
PRODUCTION DRAWING 372223

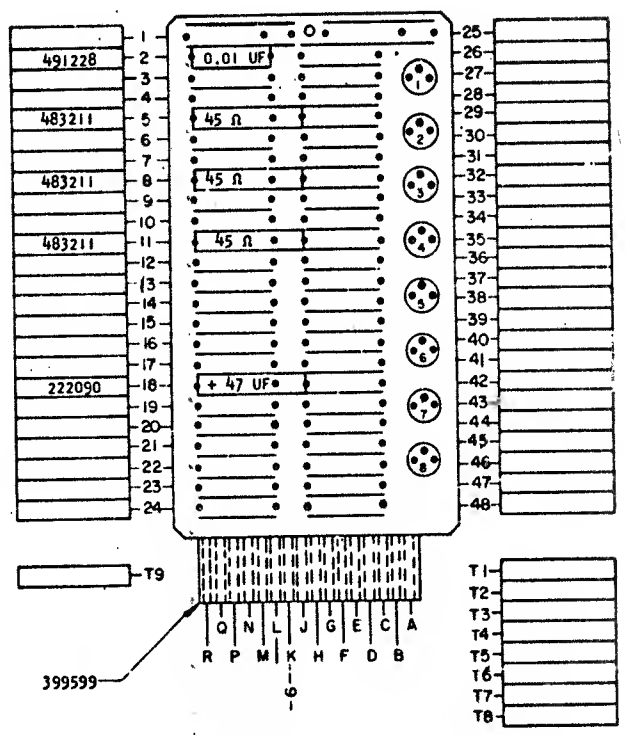
SET/RESET LOAD



APPLICATION

USED TO LIMIT THE DRIVE CURRENT TO THE SWITCH CORE MATRIX.





COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.														
NAME	SET/RESET LOAD						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734395
							3-25-63	116800						
DESIGN			MODEL	SMS 1440										
DETAIL			SCALE	NONE										
CHECK			DRAW	MOE	2-20-63									
APPRO		3-25-63	CHECK											

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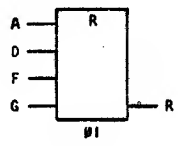
YKV–

P/N: 372224 EC: 0114426

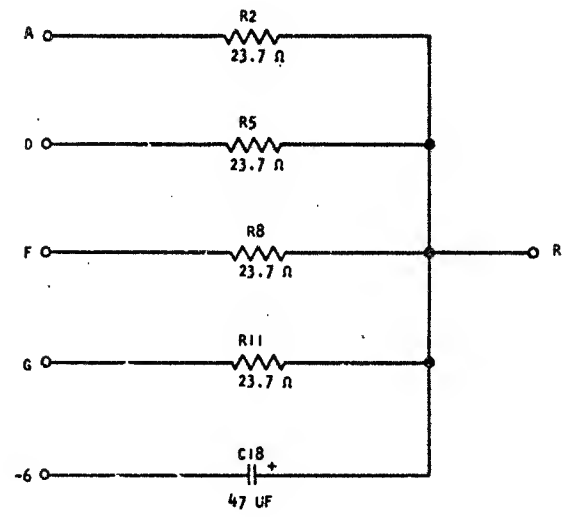
REFERENCE DRAWING
PRODUCTION DRAWING 372224

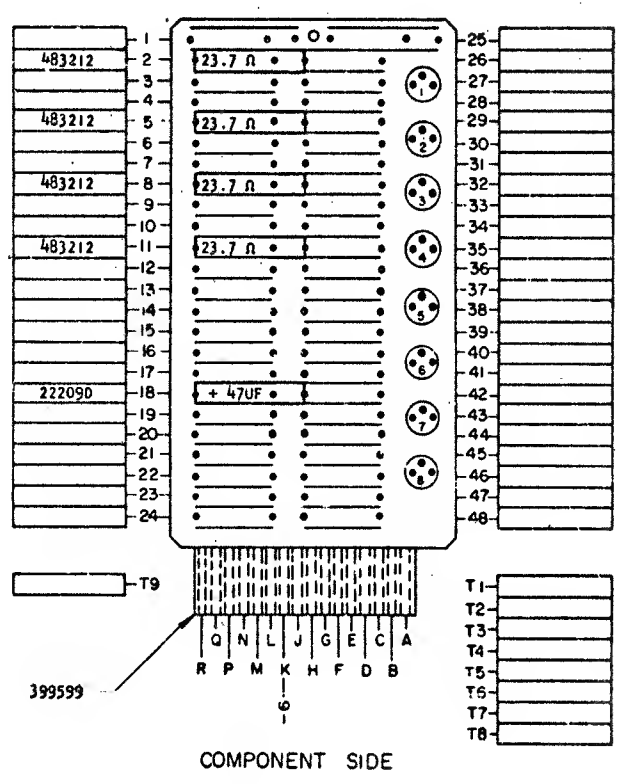
INHIBIT LOAD



APPLICATION

USED TO LIMIT THE AMOUNT OF INHIBIT CURRENT DRAWN FROM THE DRIVER THROUGH THE INHIBIT WINDING OF ONE MEMORY PLANE.





COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	INHIBIT LOAD				3-25-63	116800					734396
DESIGN			MODEL	SMS 1440							
DETAIL			SCALE	NONE							
CHECK			DRAW	HDE 2-21-63							
APPRD	[illegible] 3-25-63		CHECK								

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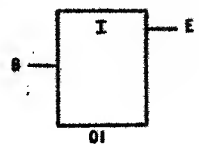
REFERENCE DRAWING
PRODUCTION DRAWING 372225

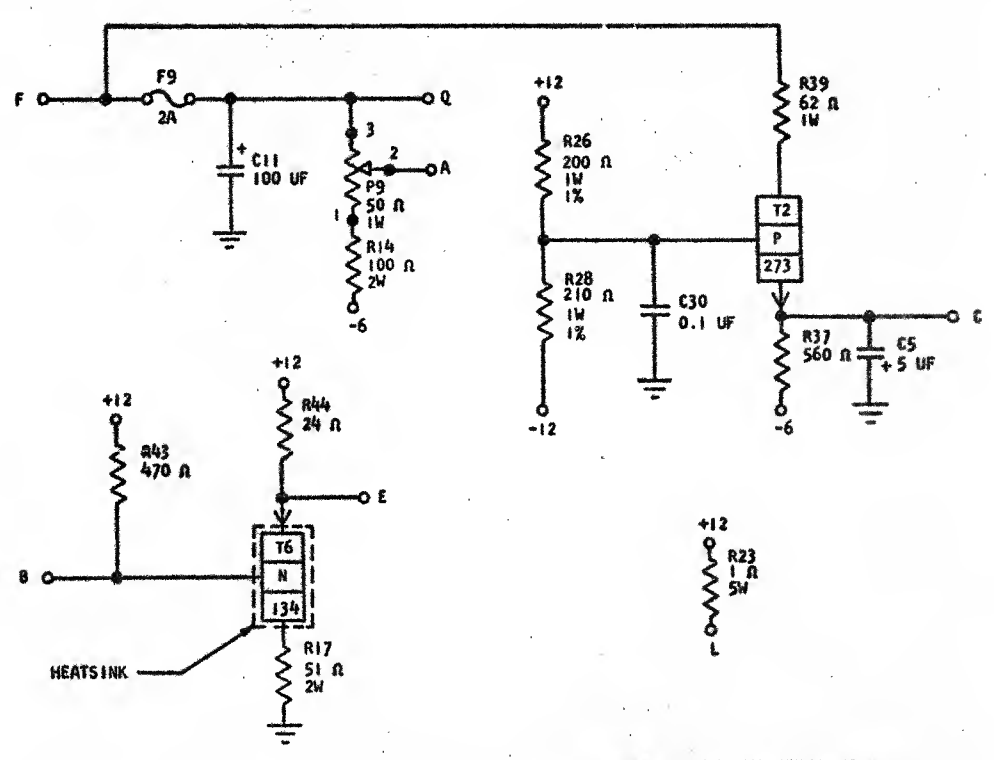
VOLTAGE REGULATOR #2

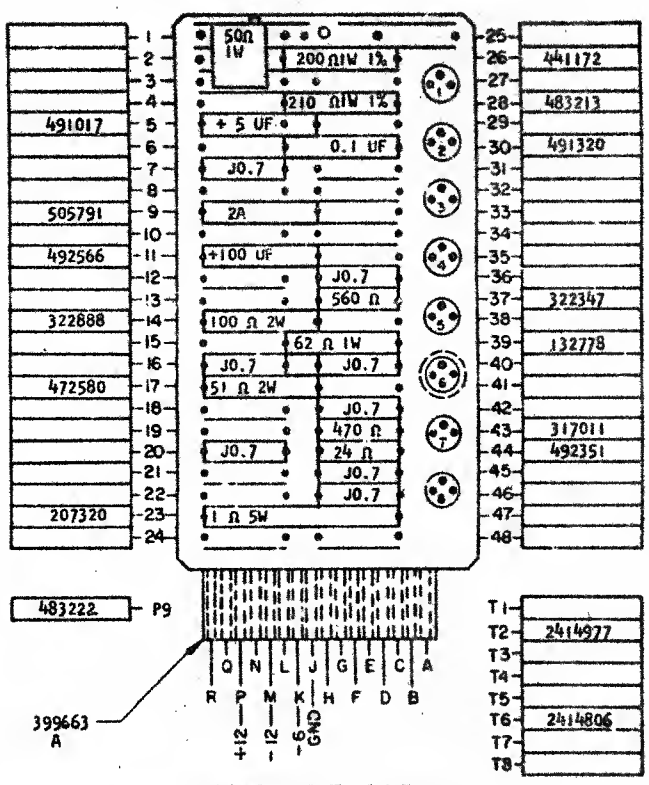


APPLICATION

CONF. 03 - OUTPUT SENSE LEVEL CIRCUIT - KEEPS THE THRESHOLD ON THE SENSE OUTPUT AMPLIFIER INSENSITIVE TO ±12 VOLT LOGIC LEVEL SHIFTS.
OUTPUT PIN C - VOLTAGE LEVELS -0.2V TO -1.2V

CONF. 01 - CONSISTS OF AN EMITTER FOLLOWER TO T6 AND IS USED TO DRIVE THE SERIES REGULATOR TRANSISTOR T5. (SEE DRAWING YKX-)





COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	VOLTAGE REGULATOR #2					3-25-63	116800						734397
						12-19-63	117838						
DESIGN			MODEL	SMS		8NOV66	130350						
DETAIL			SCALE	NONE									
CHECK			DRAW	MDE	2-21-63								
APPRO		3-25-63	CHECK										

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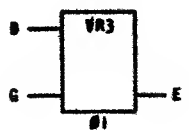
P/N: 372226

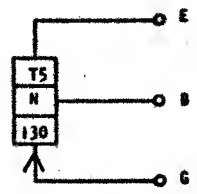
REFERENCE DRAWING
PRODUCTION DRAWING 372226

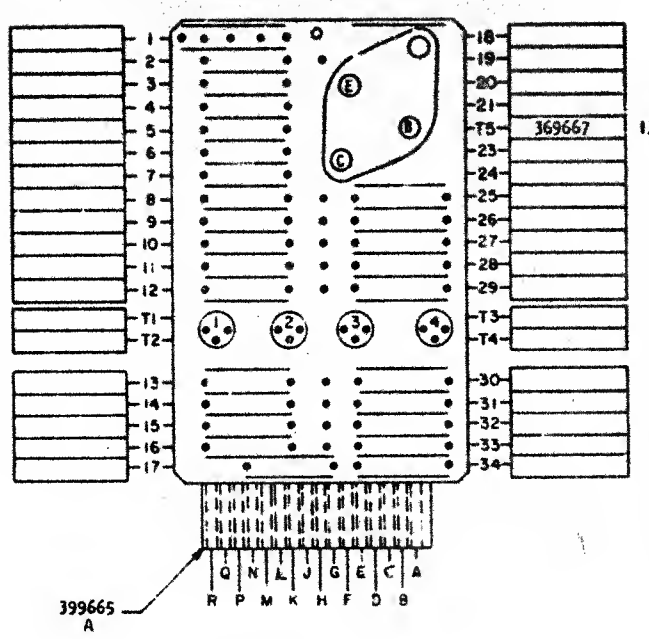
VOLTAGE REGULATOR #3



APPLICATION

USED TO DRIVE THE REGULATOR LOAD





COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734398
NAME	VOLTAGE REGULATOR #3					3-25-63	116800						
						5-11-65	123738	GLK					
DESIGN			MODEL	SMS 1440									
DETAIL			SCALE	NONE									
CHECK			DRAW	HDE	2-21-63								
APPRO	[illegible]	3-25-63	CHECK										

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2 of 1

734399

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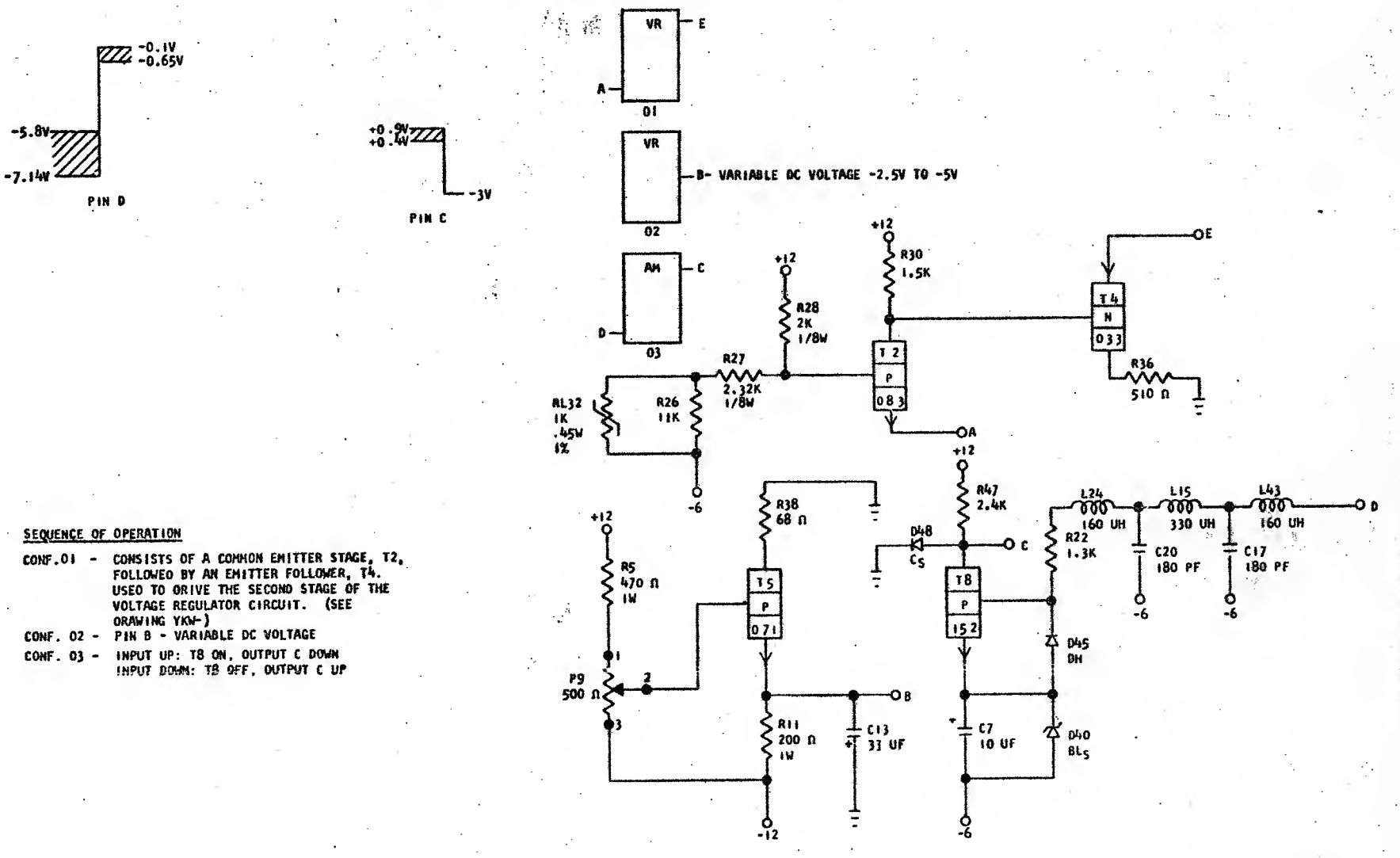
P/N: 372227

REFERENCE DRAWING
PRODUCTION DRAWING 372227

PARTIAL VOLTAGE REGULATOR AND SENSE GATE GEN.

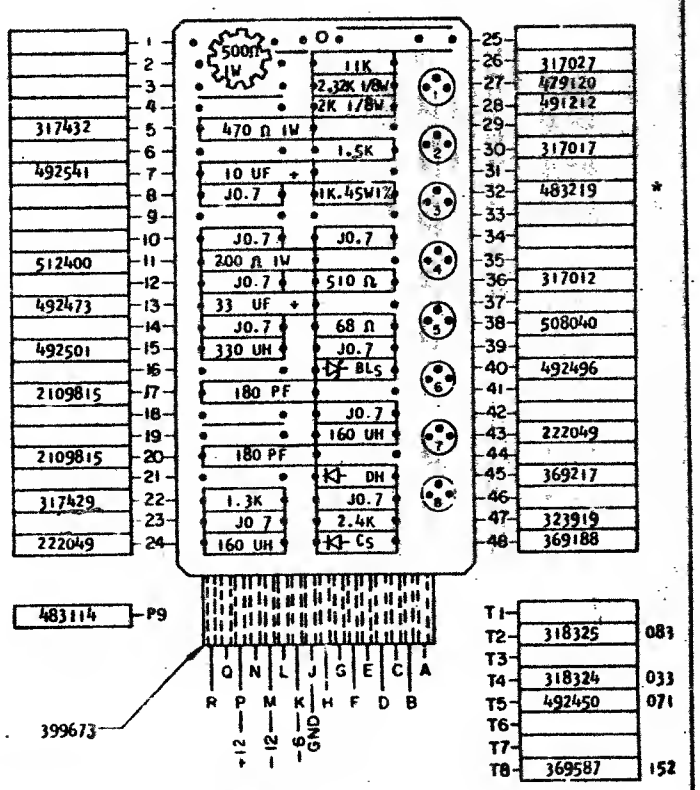


SEQUENCE OF OPERATION

CONF. 01 - CONSISTS OF A COMMON EMITTER STAGE, T2, FOLLOWED BY AN EMITTER FOLLOWER, T4. USED TO DRIVE THE SECOND STAGE OF THE VOLTAGE REGULATOR CIRCUIT. (SEE DRAWING YKW-)

CONF. 02 - PIN B - VARIABLE DC VOLTAGE

CONF. 03 - INPUT UP: T8 ON, OUTPUT C DOWN
INPUT DOWN: T8 OFF, OUTPUT C UP



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	734399
NAME	PARTIAL VOLTAGE REGULATOR AND SENSE GATE GEN.				3-25-63	116800						
					11-5-63	118939						
DESIGN			MODEL	SMS 1440	7-1-64	119012-B						
DETAIL			SCALE	NONE								
CHECK			DRAW	MDE 2-21-63								
APPRO	3-25-63		CHECK									

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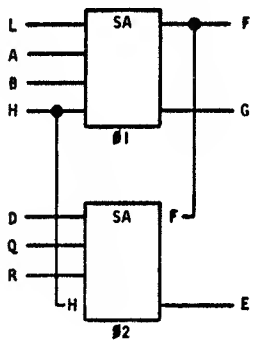
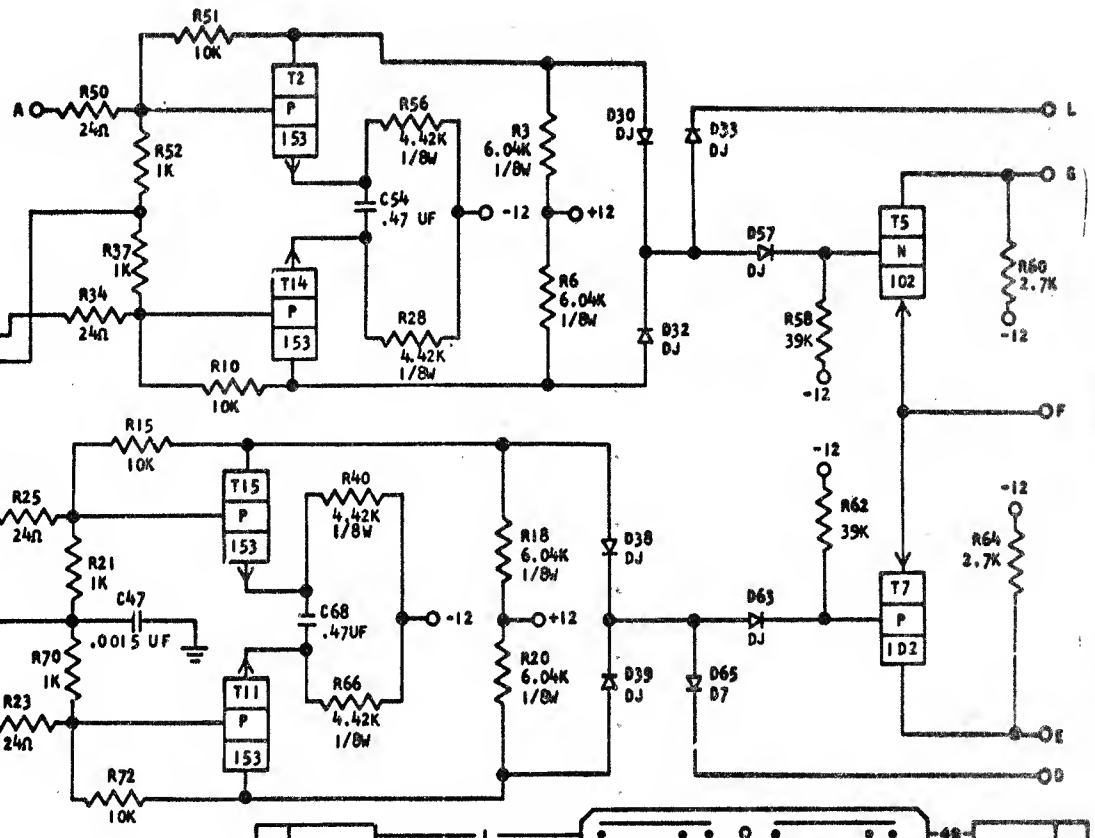
P/N: 372229

REFERENCE DRAWING
PRODUCTION DRAWING 372229

SENSE AMPLIFIER





SEQUENCE OF OPERATION

1. SENSE INPUT AMPLIFIER CONSISTS OF A DIFFERENTIAL AMPLIFIER. THE INPUT SIGNAL IS RECTIFIED TO THE SENSE AMPLIFIER T5 OR T7 IF PIN L OR D IS UP. T5 OR T7 IS OFF AND THE OUTPUT IS DOWN.

2. WHEN PIN L OR D IS DOWN, SIGNAL IS IGNORED, T5 OR T7 IS ON AND THE OUTPUT IS UP.

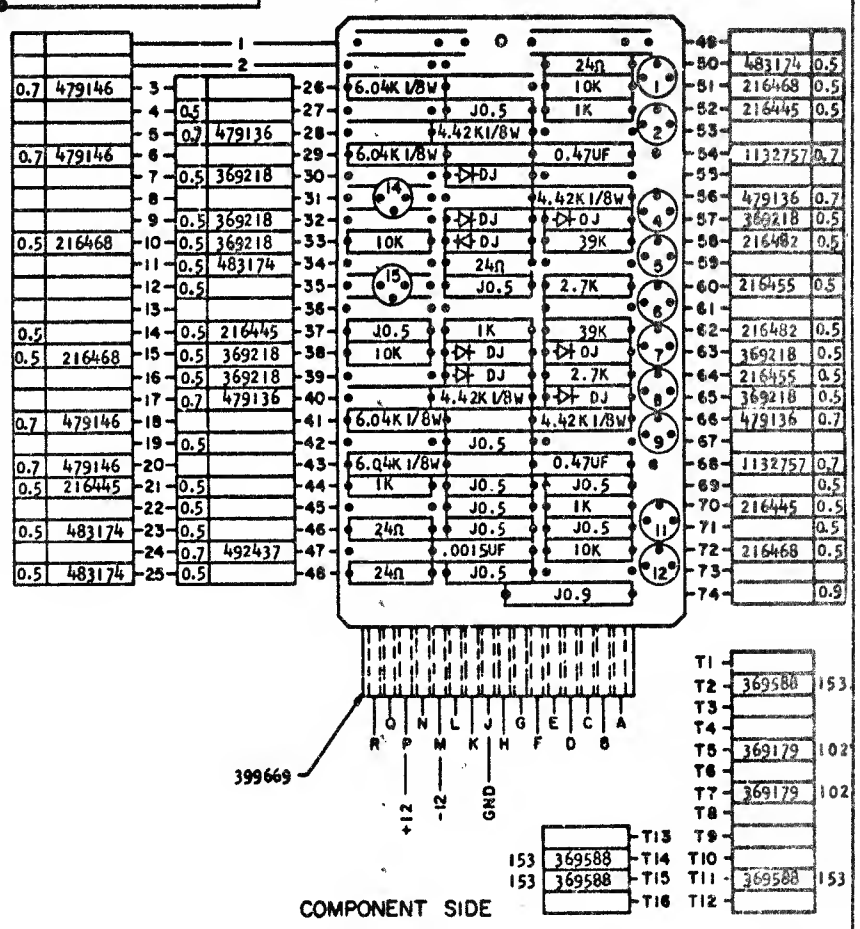
PINS	SIGNAL NAME	WAVESHAPE	LEVELS		
L,D	VSG SENSE GATE VOLTAGE		UP	+0.5V	
			DOWN	-3.0V	
A,B Q,R	INPUT		30-50 MV CORE OUTPUT		
G,E	OUTPUT			MIN	MAX
			UP	-1.7V	-0.2V
			DOWN	-5.76V	-6.91V
				-11.52V	-12.48V
H	VSL SENSE LEVEL VOLTAGE	VARIABLE D-C LEVEL	-2V TO -3V		
F	VOSL OUTPUT SENSE LEVEL	VARIABLE D-C LEVEL	-0.2V TO -1.2V		

[1] 3K LOAD TO GROUND

[2] NO LOAD

DELAY

TOTAL DELAY THRU THE CIRCUIT IS APPROXIMATELY 200 NSEC.



INTERNATIONAL BUSINESS MACHINES CORP.														
NAME	SENSE AMPLIFIER													
DESIGN			MODEL											
DETAIL			SCALE	NONE										
CHECK			DRAW	MOE	2-21-63									
APPRD	KEH	3-25-63	CHECK											

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
3-25-63	116800					
6-18-64	120095-A	FVL				
10-23-64	121908	GLK				
18DEC67	132189					
16FEB68	132520					

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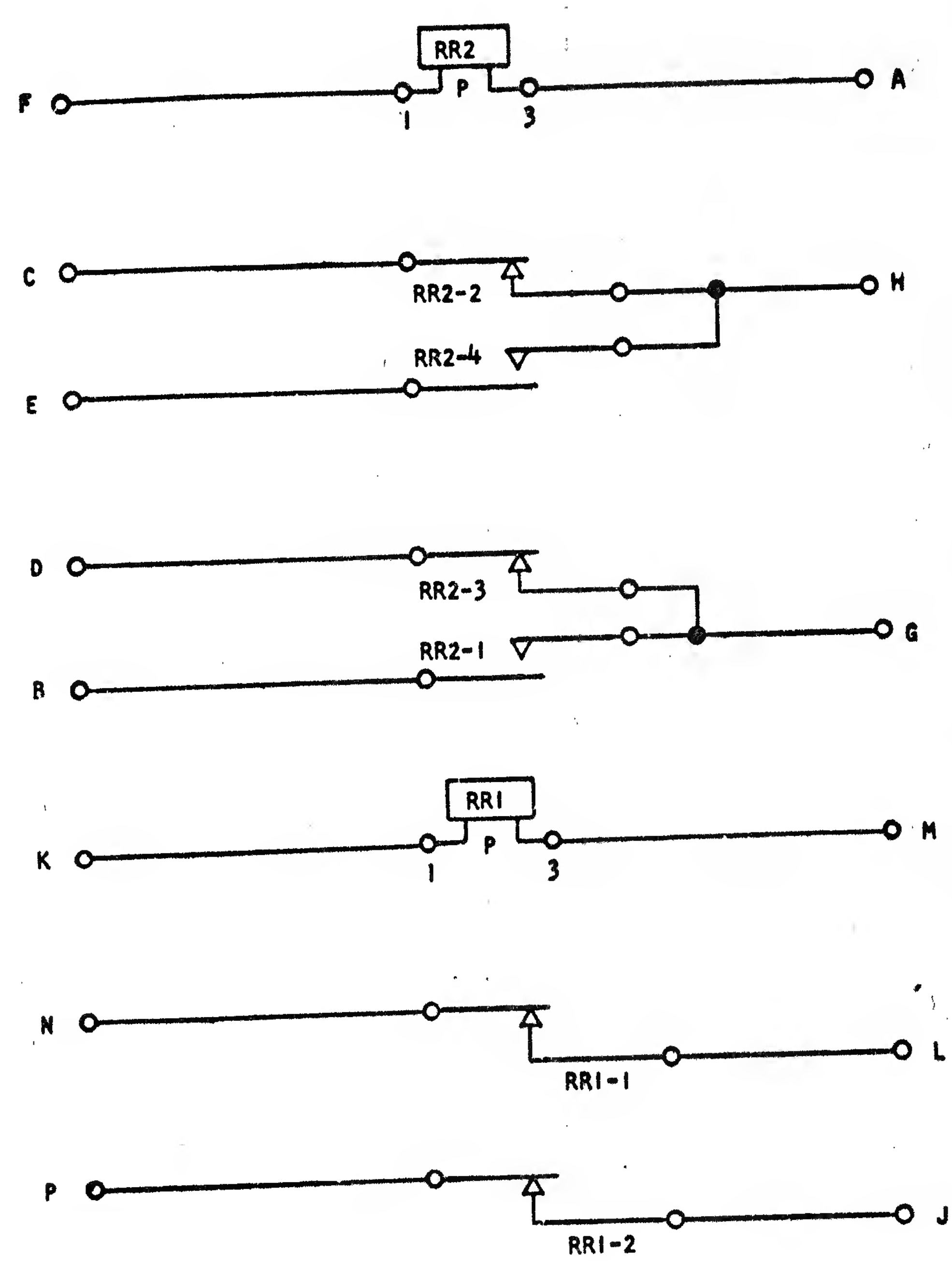
372680	Y P M -
STANDARDS CODE	2-7045

REED RELAY



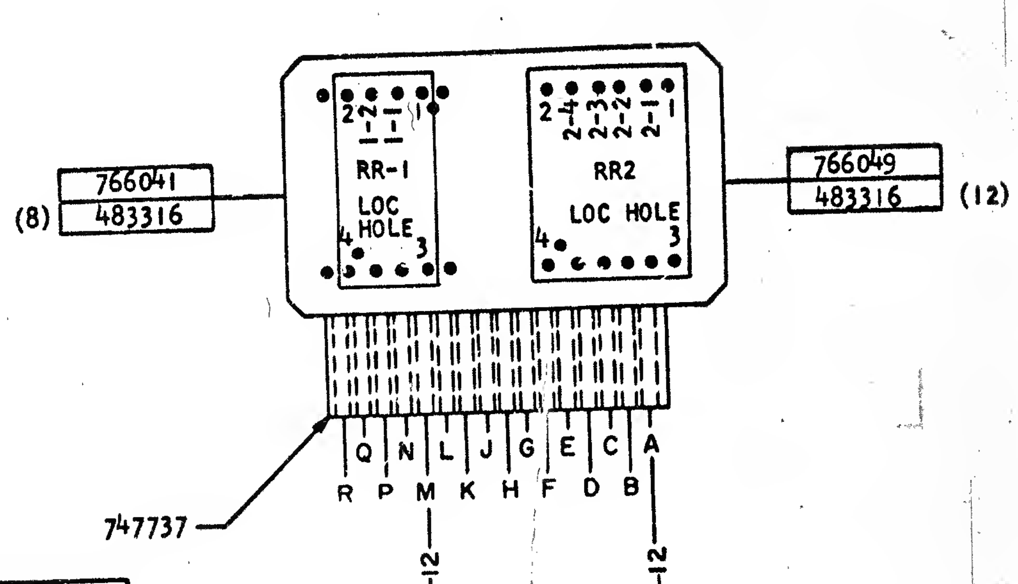
NOTES

X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION

XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999 AND 892058

XII REED RELAY ASSEMBLIES MUST NOT BE SUBJECTED TO LIQUIDS

XIII SLOT IN LUG (483316) MUST BE PARALLEL TO X-X AXIS



COMPONENT SIDE

B

PW 22NOV67

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
KMT (NPB)	8-22-63

HOLE PATTERN
747853

INTERNATIONAL BUSINESS MACHINES CORP.

NAME	CARD ASM TSTR- REED RELAY		
DESIGN	CC	4-63	MODEL	
DETAIL	JA	5-63	SCALE	NONE
CHECK	TZA	5-63	DRAW	ENS 1-21-
APPRO	WJR	8-63	CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL
3-10-64	115976	GWS			
10DEC65	D126162	GLK			
4DEC67	132195	GWS			

DEVELOPMENT NO.
PA-2825
CIRCUIT FAMILY

372680

822942

STANDARDS CODE 2-7045

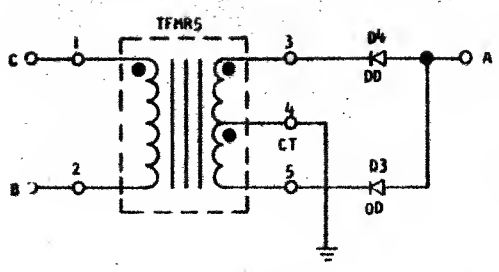
CARD CODE YYA- 822942

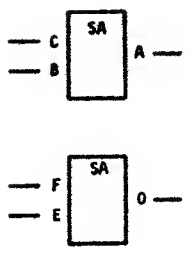
REFERENCE DRAWING

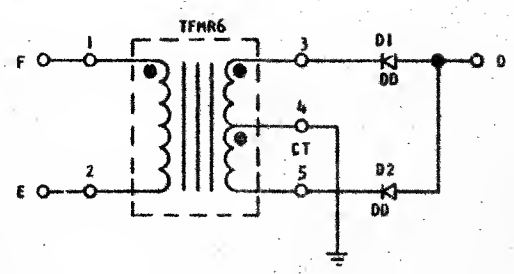
SEE PRODUCTION DRAWING 372701
AT EC LEVEL 117889

CORE INTERFACE

RECOMMEND MOUNTING ON ONE INCH CENTER
NOTE XIII



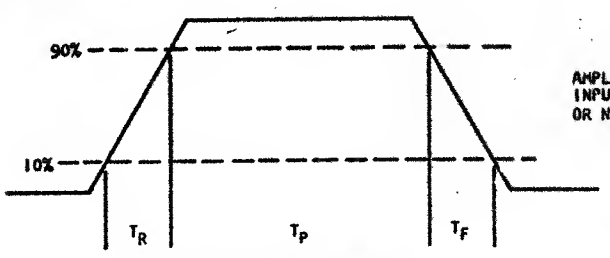




CIRCUIT OPERATION:

1. A PUSITIVE PULSE APPLIED TO INPUT GIVES A NEGATIVE PULSE AT THE OUTPUT.
2. A NEGATIVE PULSE APPLIED TO THE INPUT GIVES A NEGATIVE PULSE AT THE OUTPUT.

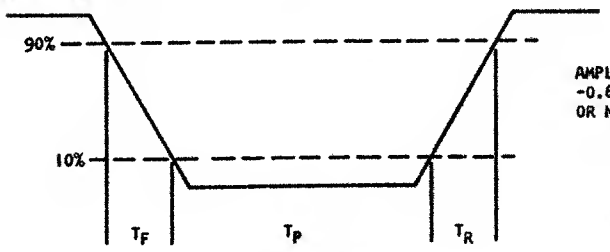
INPUT WAVEFORM:



AMPLITUDE = 0.09V TO 0.11V PEAK
INPUT WAVEFORM MAY BE A POSITIVE OR NEGATIVE PULSE.

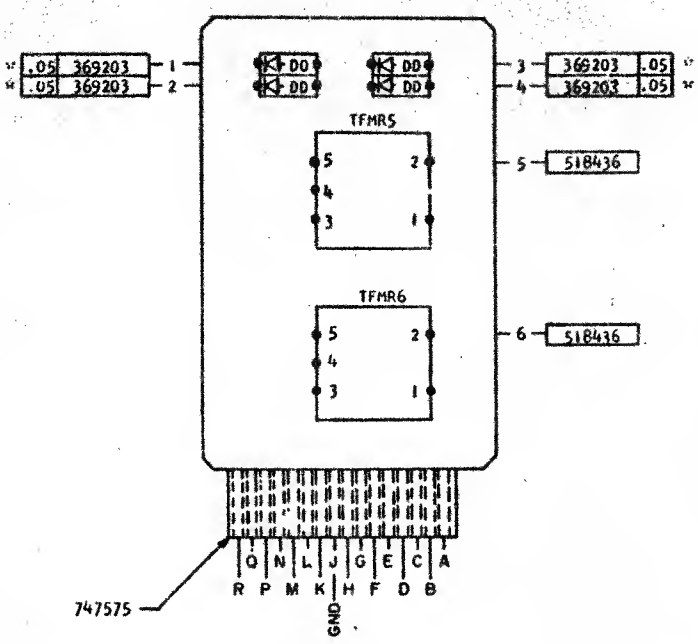
T_R = 150 TO 250 NANOSECONDS
T_P = 3 MICROSECONDS
T_F = 200 TO 300 NANOSECONDS

OUTPUT WAVEFORM:



AMPLITUDE EQUAL TO OR GREATER THAN -0.6 VOLTS WITH INPUT POSITIVE OR NEGATIVE

T_F = 150 TO 250 NANOSECONDS
T_P = 3 MICROSECONDS
T_R = 200 TO 300 NANOSECONDS



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
BC	4-13-64

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CORE INTERFACE				6-2-64	121287					
DESIGN			MODEL	SMS - 1444							
DETAIL			SCALE	NONE							CIRCUIT FAMILY
CHECK			DRAW	LIG 4-7-64							SDTDL
APPRO			CHECK	EMS 5-18-64							

822942

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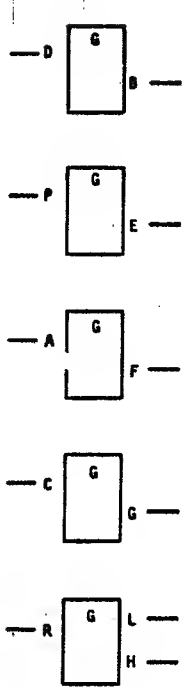
STANDARDS CODE
2-7045

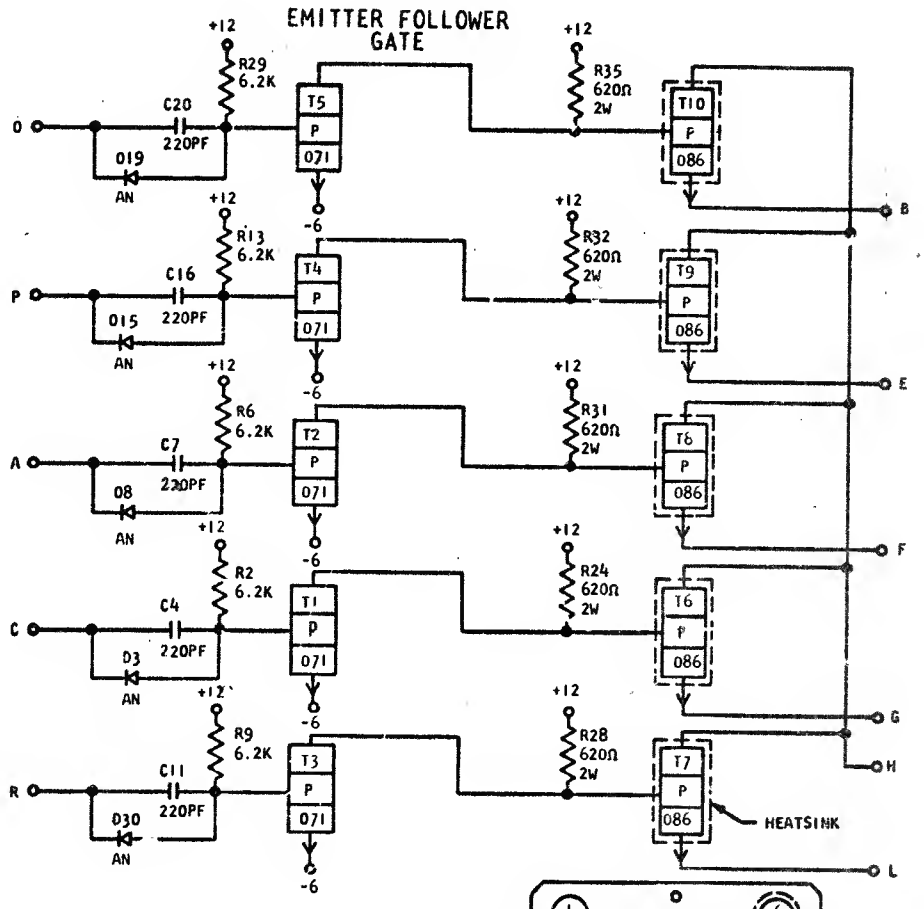
822940

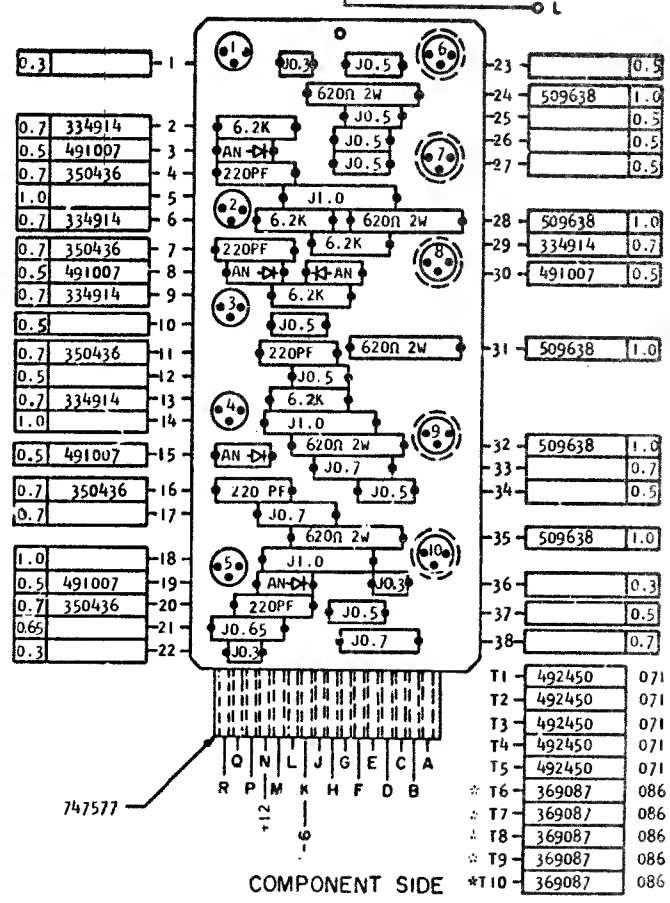
CARD CODE	822940
Y Y 8 -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 372702
AT EC LEVEL 117890







CIRCUIT OPERATION:

1. INPUT DOWN, OUTPUT TRANSISTOR IS ON, OUTPUT LEVEL IS UP.
2. INPUT UP, OUTPUT TRANSISTOR IS OFF, OUTPUT IS OPEN CIRCUIT.
3. PIN H IS TO BE TIED THROUGH A RESISTOR TO A VOLTAGE.
   INPUT UP, H IS UP
   INPUT DOWN, H IS DOWN

PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D,P A,C R	INPUT		UP	-4.66	+0.24
			DOWN	-6.94	-12.48
B,E F,G L	OUTPUT		UP		+1.92
			DOWN	OUTPUT OPEN CIRCUIT	
H	OUTPUT		UP	+11.52	+12.48
			DOWN		+2.42

NOTE: THE LEVELS AT THE OUTPUT DEPEND ON COLLECTOR AND EMITTER LOADING. THE GIVEN VALUES ARE FOR A COLLECTOR RETURNED TO +12 VOLTS THROUGH A 40Ω RESISTOR AND AN EMITTER LOAD REQUIRING 300 MA DRIVE CURRENT.

DELAYS - USEC

	MAXIMUM
T_{ON}	0.9
T_{OFF}	0.35

NOTE: ALL THE ABOVE DELAYS ARE MEASURED FROM -6 VOLT LEVEL ON THE INPUT TO THE -6 VOLT LEVEL ON PIN H.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-13-64

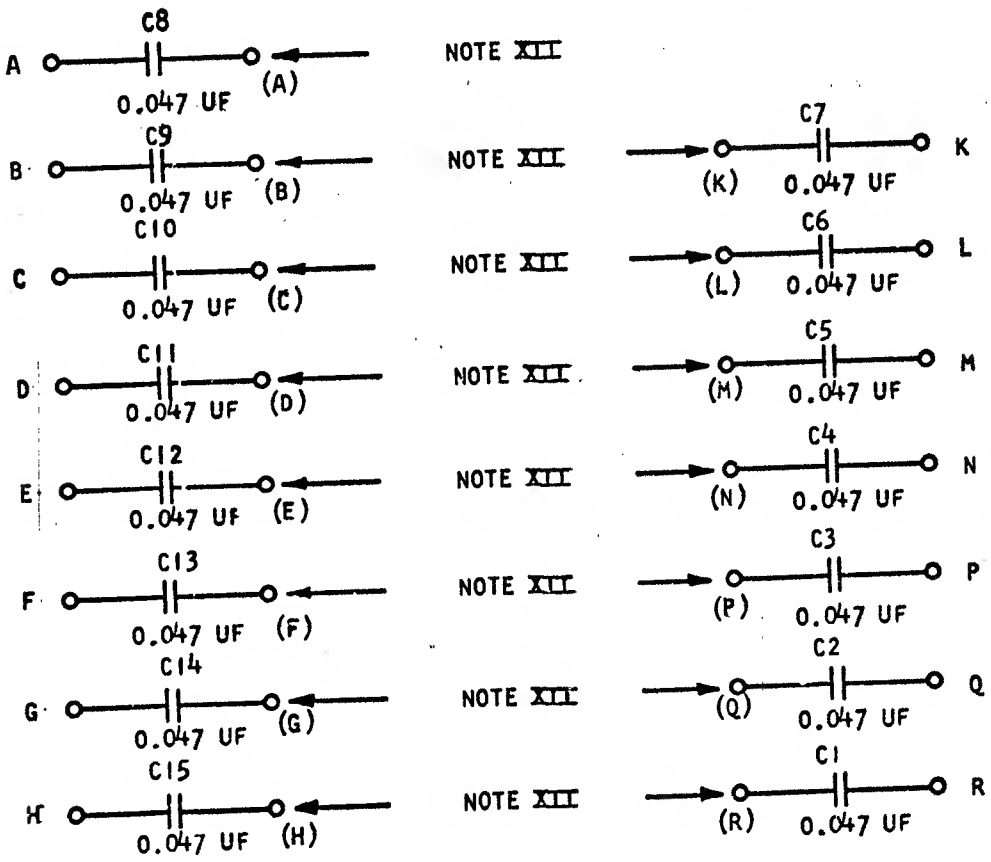
INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	822940
NAME	CARD ASM TSTR- EMITTER FOLLOWER GATE				6-2-64	121287						
DESIGN			MODEL	SMS-1444								
DETAIL			SCALE	NONE								
CHECK			DRAW	LIG 4-7-64							CIRCUIT FAMILY	
APPRO			CHECK	EWS 5-18-64							SOTOL	

C

372719

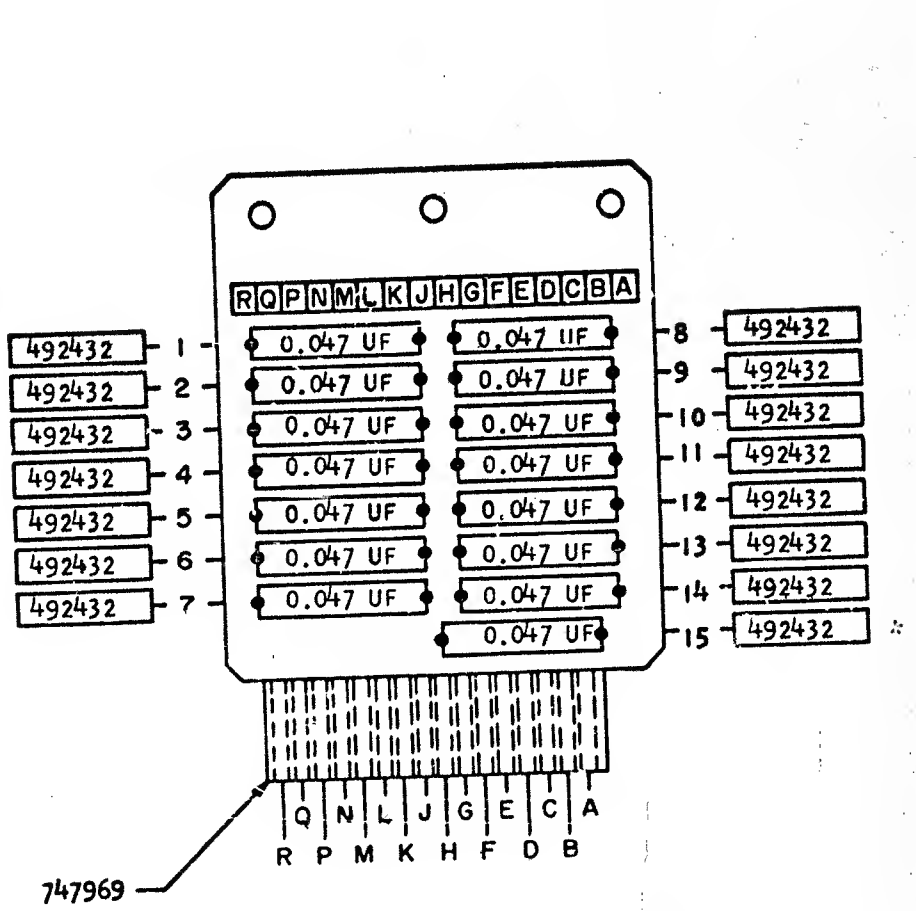
CAPACITOR CABLE CARD

STANDARDS CODE	2-7045
372719	YYC-



NOTES

- X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION
- XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
- XII CABLE ENTRY
- XIII DO NOT APPLY PROTECTIVE COATING TO WIRING SIDE.
- XIV
- XV



B

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
TBH	10-2-63

HOLE PATTERN 399366

COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.

NAME	CARD ASM STR-		
	CAPACITOR CABLE CARD		
DESIGN		MODEL	SMS 1401
DETAIL		SCALE	NONE
CHECK		DRAW	VE 10-1-63
APPRO	TBH 10-2-63	CHECK	GWS 10/1/63

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
10-8-63	118936	TBH				
4-2-64	120112	GWS				
						CIRCUIT FAMILY
						NAND

372719

FORM 85-6888-1

C.B.CO., NO. 376W 41508

822938

STANDARDS CODE 2-7045

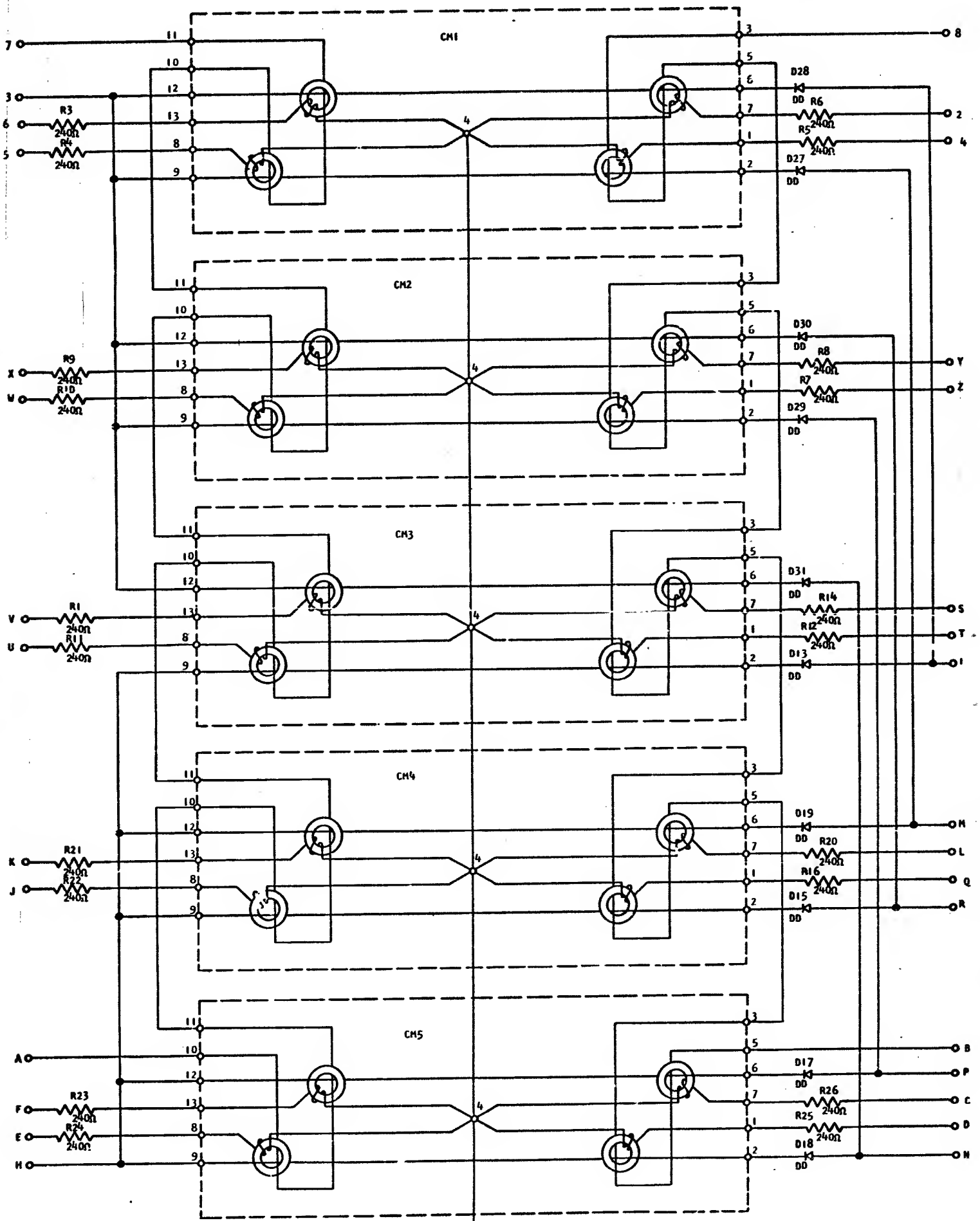
CARD CODE 822938

Y Y D-

REFERENCE DRAWING

SEE PRODUCTION DRAWING 373432
AT EC LEVEL 125829

SHEET 1 OF 3



CIRCUIT ANN PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-13-64

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	TWIN CARD ASM - CORE					6.2.64	121287						822938
	MATRIX CARD					28SEP65	125829						
DESIGN			MODEL	SMS-1444									
DETAIL			SCALE	NONE								CIRCUIT FAMILY	
CHECK	FVL	12-17-63	DRAW	LIG	10-9-63							SDTDL	
APPRO	[illegible]	12-20-63	CHECK	EAS	5-18-64								

C

822938

STANDARDS CODE 2+7045

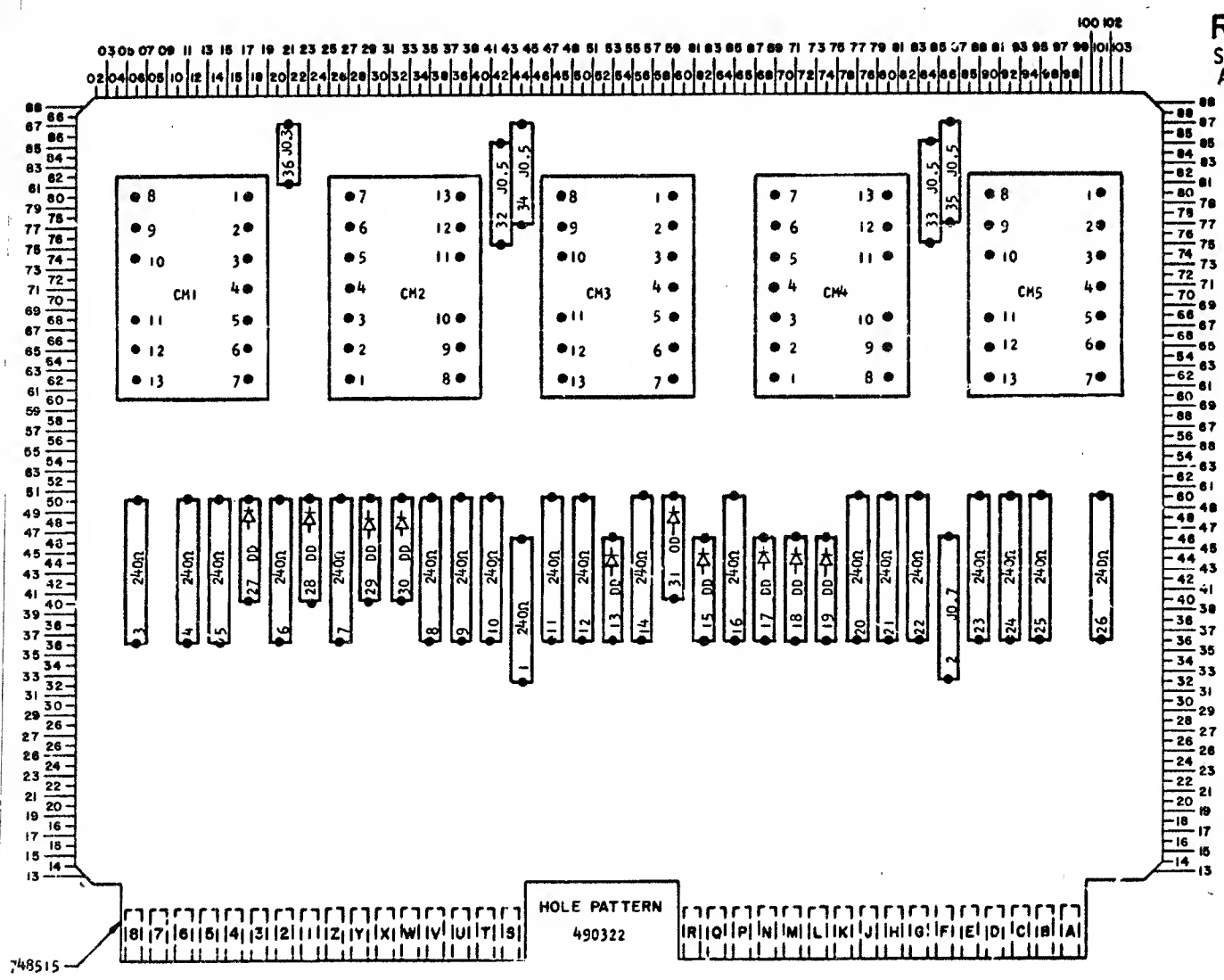
CARD CODE 822938

Y Y D -

SHEET 2 OF 3

REFERENCE DRAWING

SEE PRODUCTION DRAWING 373432
AT EC LEVEL 125829



CIRCUIT AND PACKAGING STANDARDS	
APPROVAL	DATE
ABC	4-13-64

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	TWIN CARD ASM- CORE				4-2-64	121287					
	MATRIX CARD				28SEP65	125829					
DESIGN			MODEL	SMS - 1444							
DETAIL			SCALE	NONE							
CHECK	FVL	12-9-63	DRAW	JAB 12-16-63							CIRCUIT FAMILY
APPRO	HW	12-20-63	CHECK	EAJS 5-18-64							SDTDL

822938

C

822938

STANDARDS CODE 2-7045

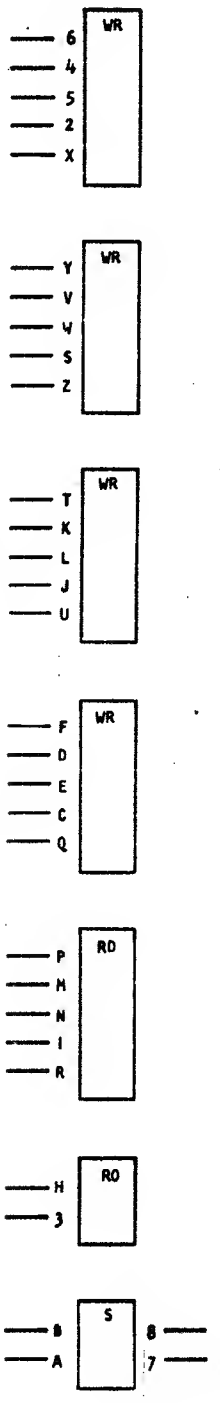
CAGE CODE 822938

Y Y D -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 373432
AT EC LEVEL 125829

SHEET 3 OF 3



CIRCUIT OPERATION:

1. RETURNING ANY WRITE INPUT TO GROUND WRITES A "1" IN A CORE WITH PIN G TIED TO -20 VOLTS.)
2. AFTER ANY READ OPERATION, THE CORE IS IN THE "0" STATE AND REMAINS THERE UNTIL A "1" IS WRITTEN BY PULSING A WRITE LINE.
3. PULSING A READ LINE READS THE STATE OF A CORE. THE STATE IS SENSED ON THE SENSE LINES.

PINS	SIGNAL NAME	WAVE SHAPE	LEVELS		
				MIN	MAX
6,4,5 Z,X,Y V,W,S Z,T,K L,J,U,C F,D,E,Q	WRITE INPUT FOR A "1"	P.W. = 500 US MIN	UP	GROUND	
			DOWN	-18.2V	-21.6V
B,A 8,7	SENSE			13 MV	

PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	
			MIN	MAX
P,M,N I,R,H 3	READ INPUT	1.5 US MIN	200 MA	300 MA
B,A 8,7	SENSE OUTPUT FOR "0"		N.A.	30 MV
B,A 8,7	SENSE OUTPUT FOR "1"		130 MV	N.A.

CIRCUIT ARD PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-13-64

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVA	DEVELOPMENT NO.	
NAME	TWIN CARD ASM - CORE MATRIX CARD					6-2-64	121287						822938
DESIGN			MODEL	SMS - 1444		28SEP65	125829						
DETAIL			SCALE	NONE									
CHECK	FV	12-19-63	DRAW	LIG	4-7-64							CIRCUIT FAMILY	
APPRO		12-20-63	CHECK	EJS	5-18 64							SOTOL	

C

2-2

STANDARDS CODE
2-7045

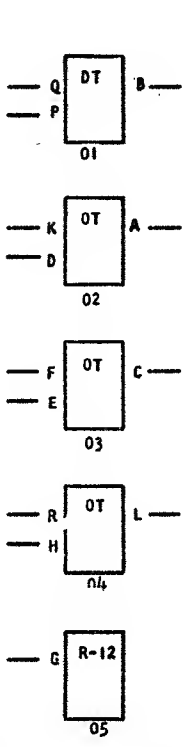
822935

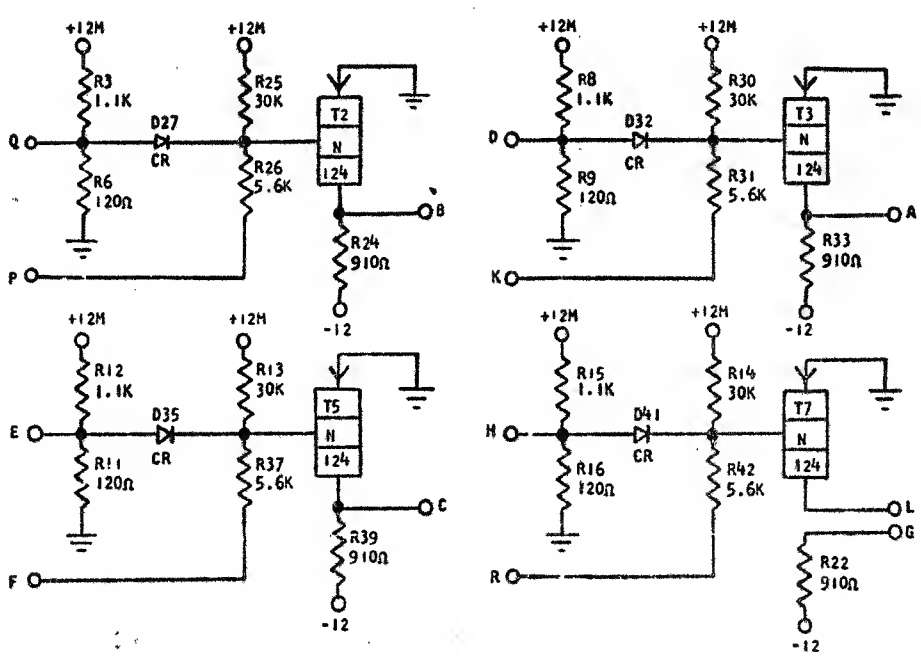
CARD CODE	822935
Y Y N -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 372723
AT EC LEVEL 119662

SDTDL/SDTRL - STANDARD INTERFACE TERMINATOR, GATED





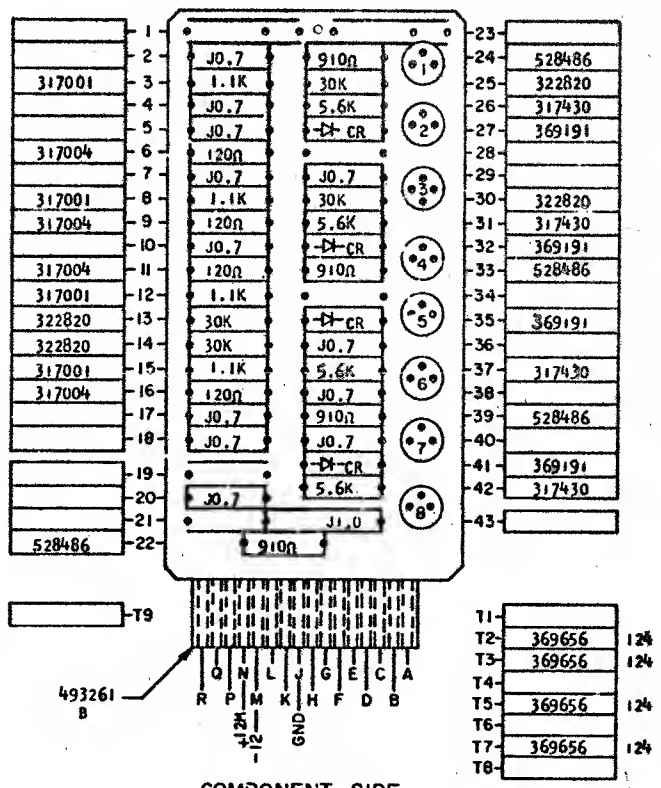
CIRCUIT OPERATION

1. LINE INPUT (PINS Q,D,E,H) HAS NO CONTROL UNLESS GATE (PINS P,K,F,R) IS AT DOWN LEVEL
2. WHEN GATE IS AT OOWN LEVEL, A OOWN LEVEL ON THE LINE INPUT CAUSES THE TRANSISTOR TO TURN ON GIVING A POSITIVE OUTPUT
3. PIN G IS A 910 Ω 1/2 WATT RESISTOR RETURNED TO -12 VOLTS AVAILABLE AS A LOAD FOR CONF. 04, OR ANY APPLICATION REQUIRING A 910 Ω RESISTOR TO -12 VOLTS.

PINS	SIGNAL NAME		WAVE SHAPE	LEVEL	MIN	MAX
Q,D E,H	C	LINE INPUT		UP	+0.55V	+3.26V
				DOWN	-0.5V	-5.3V
P,K F,R		GATE INPUT		UP	-0.80V	+1.68V
				DOWN	-5.3V	-10.8V
B,A C,L		OUTPUT		UP	-0.05V	-0.45V
				OOWN	-5.81V	-12.48V

DELAY

	MAX
TURN ON (NSEC)	65
TURN OFF (NSEC)	95



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-23-64

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR -SDTDL/SDTRL- STD INTERFACE TERMINATOR GATED				6-23-64	121287					
DESIGN			MODEL	SMS-1444							
DETAIL			SCALE	NONE							
CHECK			DRAW	LIG 4-16-64							CIRCUIT FAMILY
APPRO			CHECK	EWS 5-18-64							SDTDL

822935

C

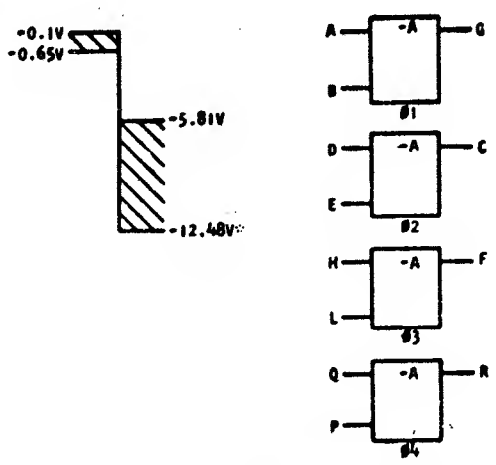
ZGG—

P/N: 372585

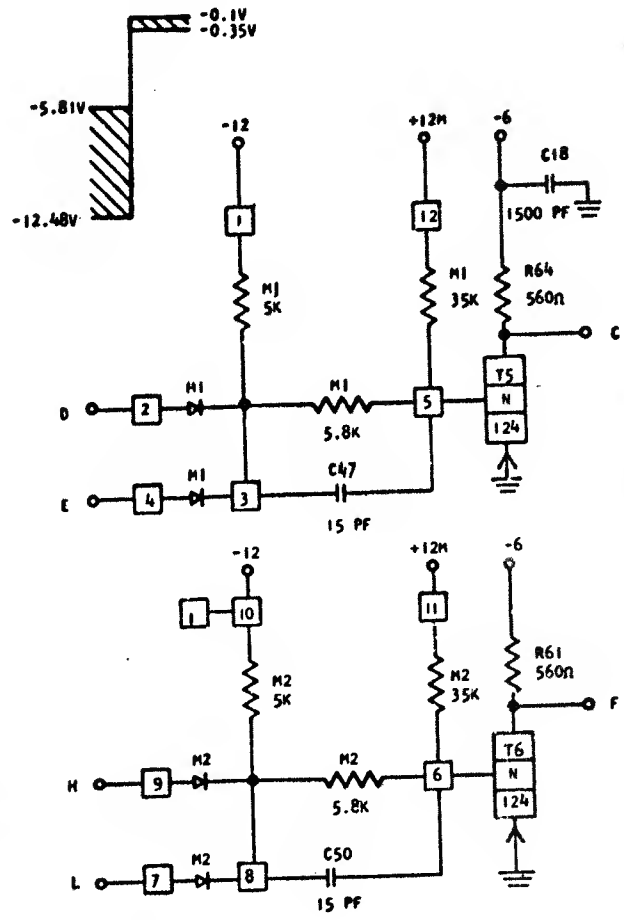
734339

REFERENCE DRAWING'
PRODUCTION DRAWING 372585

SDTDL HS FOUR 2-WAY NEGATIVE AND LOGIC BLOCKS WITH LOADS



* FUNCTION OF LOAD



OTHER DESIGNATIONS

+0, -A0, +0A, +00, I, ID, IA

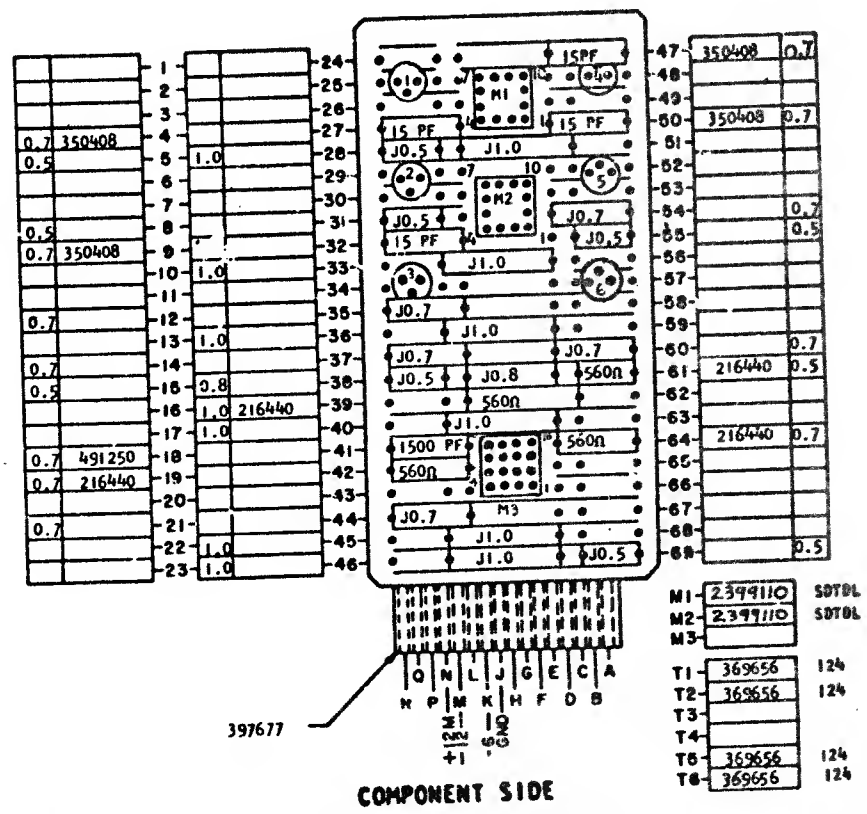
SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP TRANSISTOR OFF, OUTPUT DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	18	100
TURN OFF (NSEC)	15	150

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL HS FOUR 2-WAY NEGATIVE AND LOGIC BLOCKS WITH LOADS				4-24-63	116800C					
DESIGN			MODEL	SMS	4-28-64	121009	GWS				
DETAIL			SCALE	NONE	24JAN66	126401D	RRK				
CHECK			DRAW	MDE 4-16-63	1APR66	126401J	GLK				
APPRO	RRK 4-24-63		CHECA			132168					

734339

C

734341

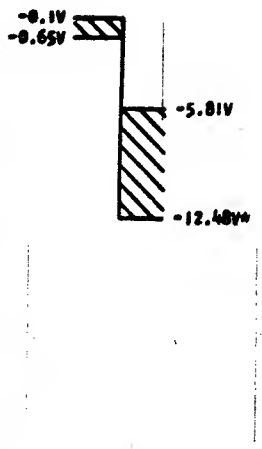
734341

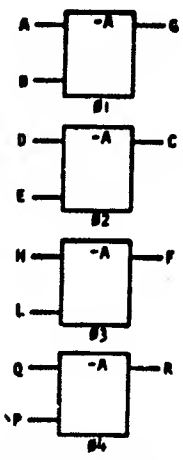
ZGH—

P/N: 372586

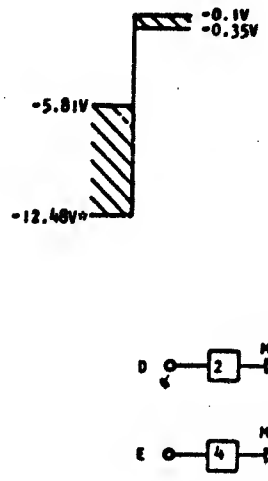
REFERENCE DRAWING
PRODUCTION DRAWING 372586

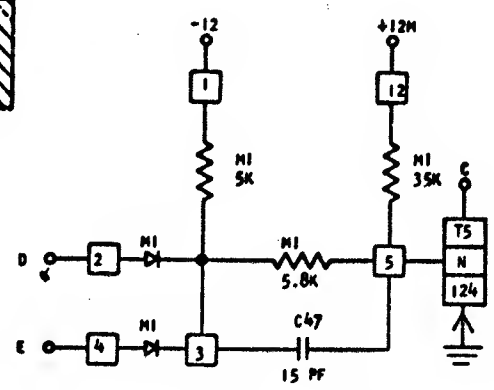
SDTDL HS FOUR 2-WAY NEGATIVE AND LOGIC BLOCKS WITHOUT LOADS

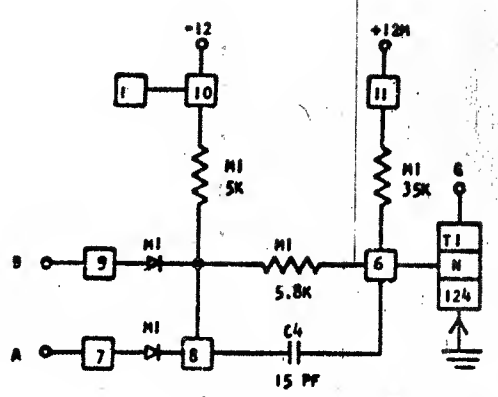


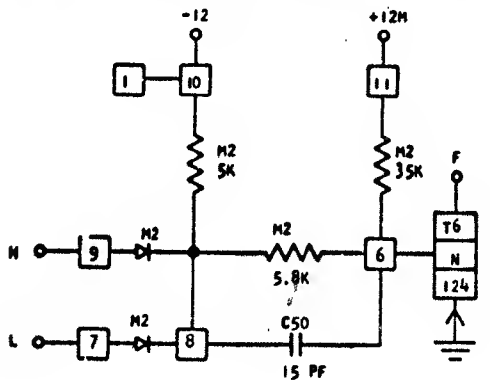


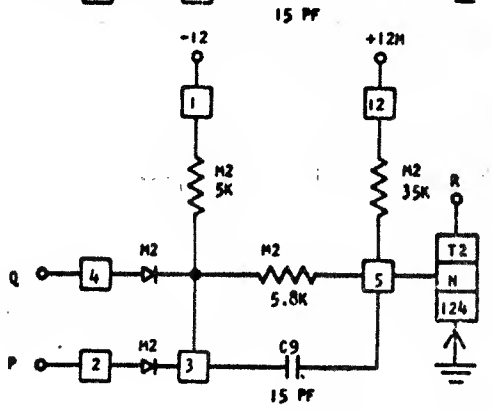
* FUNCTION OF LOAD











OTHER DESIGNATIONS

+0, -A0, +0A, +00, I, ID, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

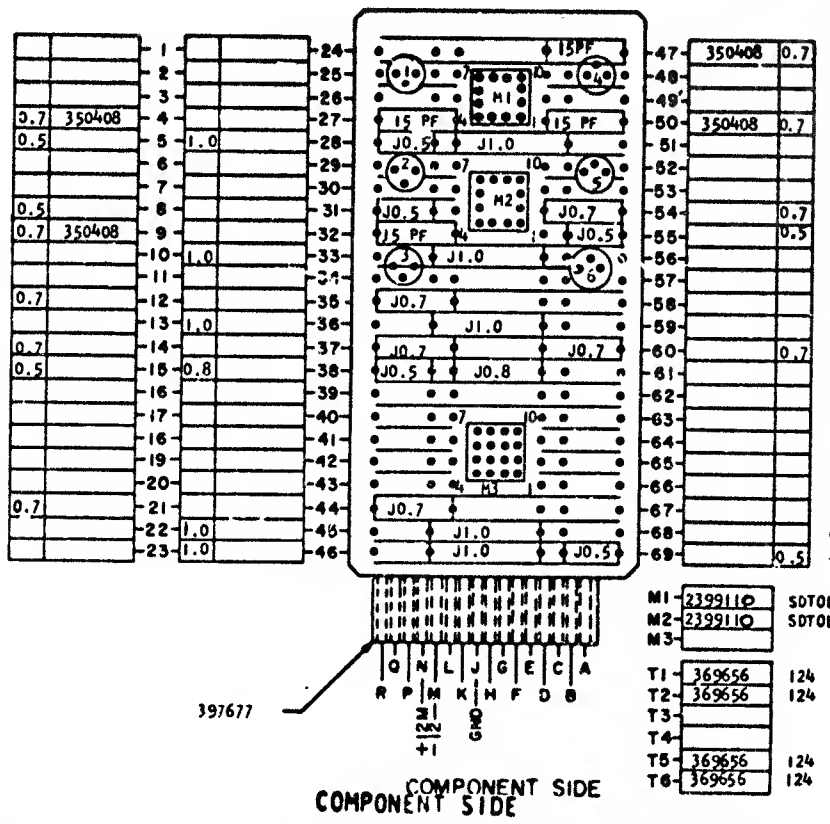
DELAY

WITH 560Ω OR 1.6K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	18	100*
TURN OFF (NSEC)	15	150**

* THIS DELAY CAN INCREASE TO 180 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.
** THIS DELAY CAN INCREASE TO 200 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.



COMPONENT SIDE

C

INTERNATIONAL BUSINESS MACHINES CORP.													
NAME	SOTOL HS FOUR 2-WAY NEGATIVE AND LOGIC BLOCKS WITHOUT LOADS						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
DESIGN			MODEL	SMS			4-24-63	116800C			132169		734341
DETAIL			SCALE	NONE			4-28-64	121009	GWS				
CHECK			DRAW	MDE	4-16-63		5-10-65	124279	GLK				
APPRO			CHECK				24JAN66	1264010					
							1APR66	1264011	GLK				

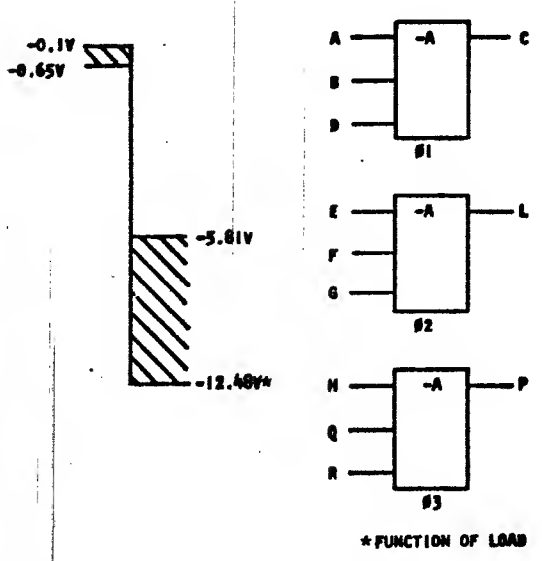
734366

STANDARDS CODE 2-6111

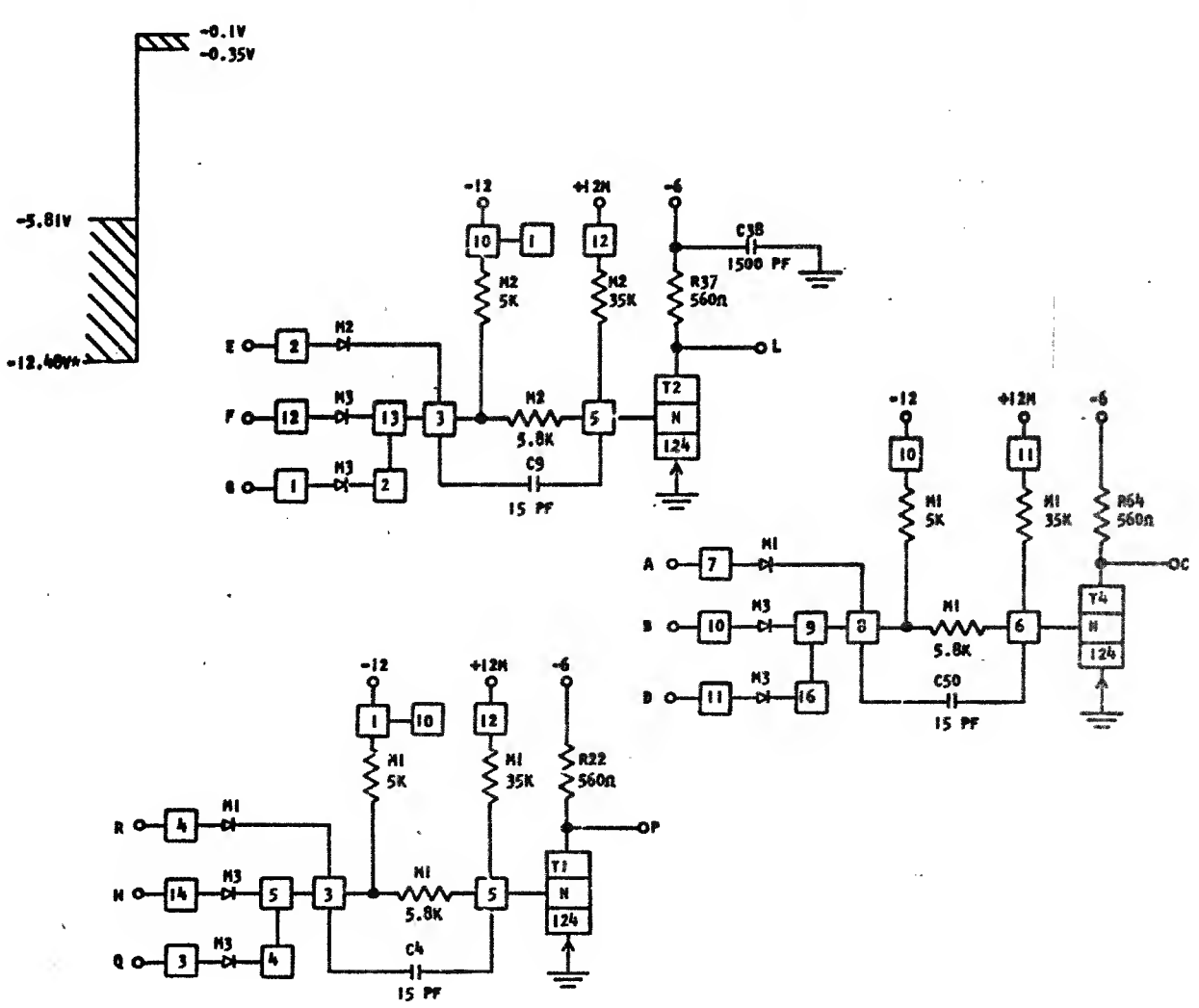
CARD CODE 734366
Z G J -

REFERENCE DRAWING
PRODUCTION DRAWING 372587

SDTDL HS THREE 3-WAY NEGATIVE AND LOGIC BLOCKS WITH LOADS



*FUNCTION OF LOAD



OTHER DESIGNATIONS

40, -A0, 40A, 400, I, ID, IA

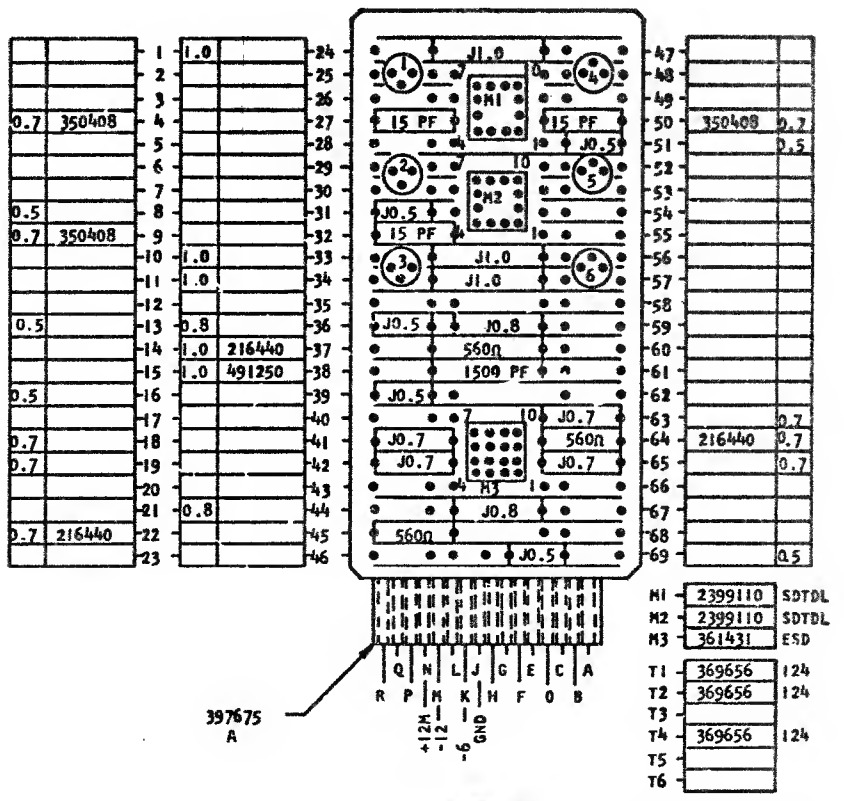
SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	18	100
TURN OFF (NSEC)	15	150

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	2APR62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	SDTDL HS THREE 3-WAY NEG. AND LOGIC BLOCKS WITH LOADS				
DESIGN	LEF	24APR68	MODEL	SMS	
DETAIL	LEF	24APR68	SCALE	NONE	
CHECK	LEF	24APR68	DRAW	LIG	5MAR68
APPRO	LEF	24APR68	CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
24APR63	116800C					
14OCT65	125832					
24JAN66	126401D	GLK				
20FEB68	132170					
12JUN68	132888	GWS				

734366

C

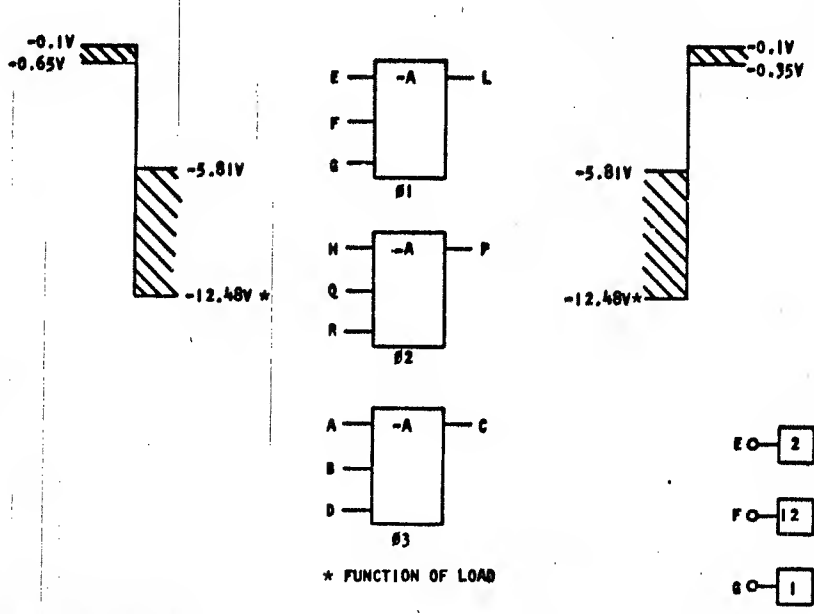
STANDARDS CODE 2-6111

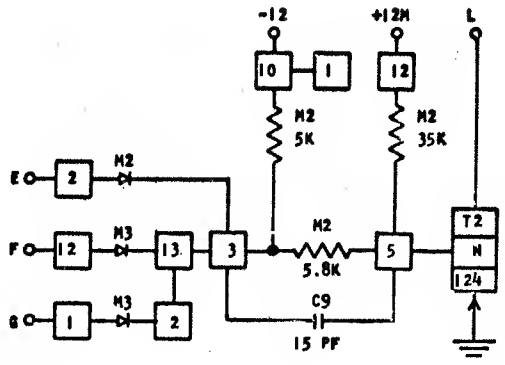
734402

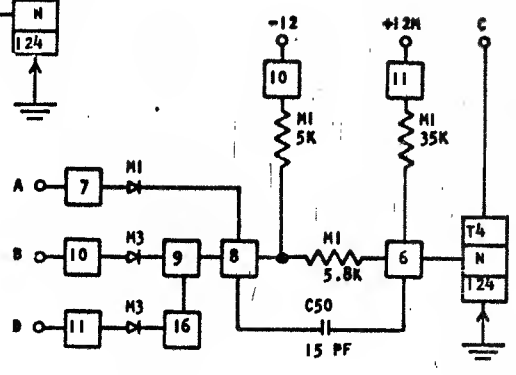
CARD CODE ZGK- 734402

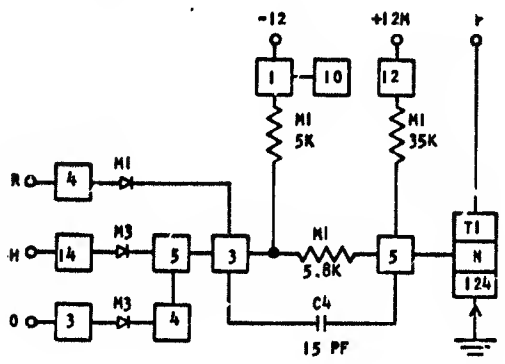
REFERENCE DRAWING
PRODUCTION DRAWING 372588

SDTDL THREE 3-WAY NEGATIVE AND LOGIC BLOCKS WITHOUT LOADS









OTHER DESIGNATIONS

+0, -A0, +0A, +00, I, ID, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

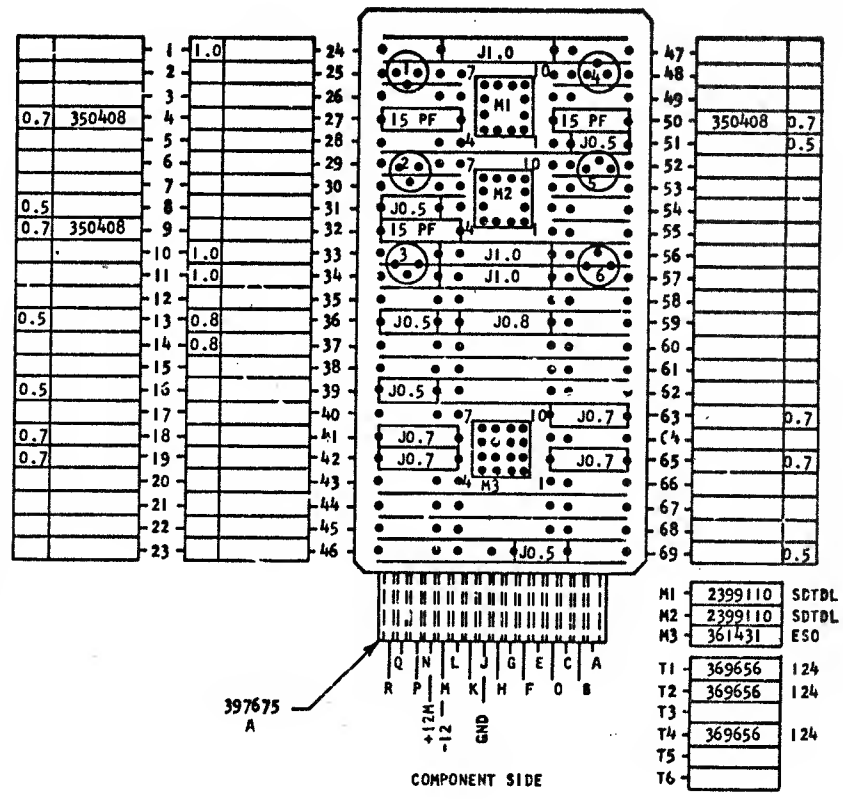
WITH 560Ω OR 1.6K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	18	100*
TURN OFF (NSEC)	15	150**

*THIS DELAY CAN INCREASE TO 180 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 200 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.



M1	2399110	SDTDL
M2	2399110	SDTDL
M3	361431	ESO
T1	369656	124
T2	369656	124
T3		
T4	369656	124
T5		
T6		

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	SDTDL THREE 3-WAY NEGATIVE AND LOGIC BLOCKS WITHOUT LOADS					24APR63	116800C						734402
DESIGN	LEF	24APR63	MODEL	SMS		14OCT65	125832						
DETAIL	LEF	24APR63	SCALE	NONE		24JAN66	126401D						
CHECK	LEF	24APR63	DRAW	LIG	5MAR68	20FEB68	132171						
APPRO	LEF	24APR63	CHECK			12JUN68	132888	GWS					

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734367

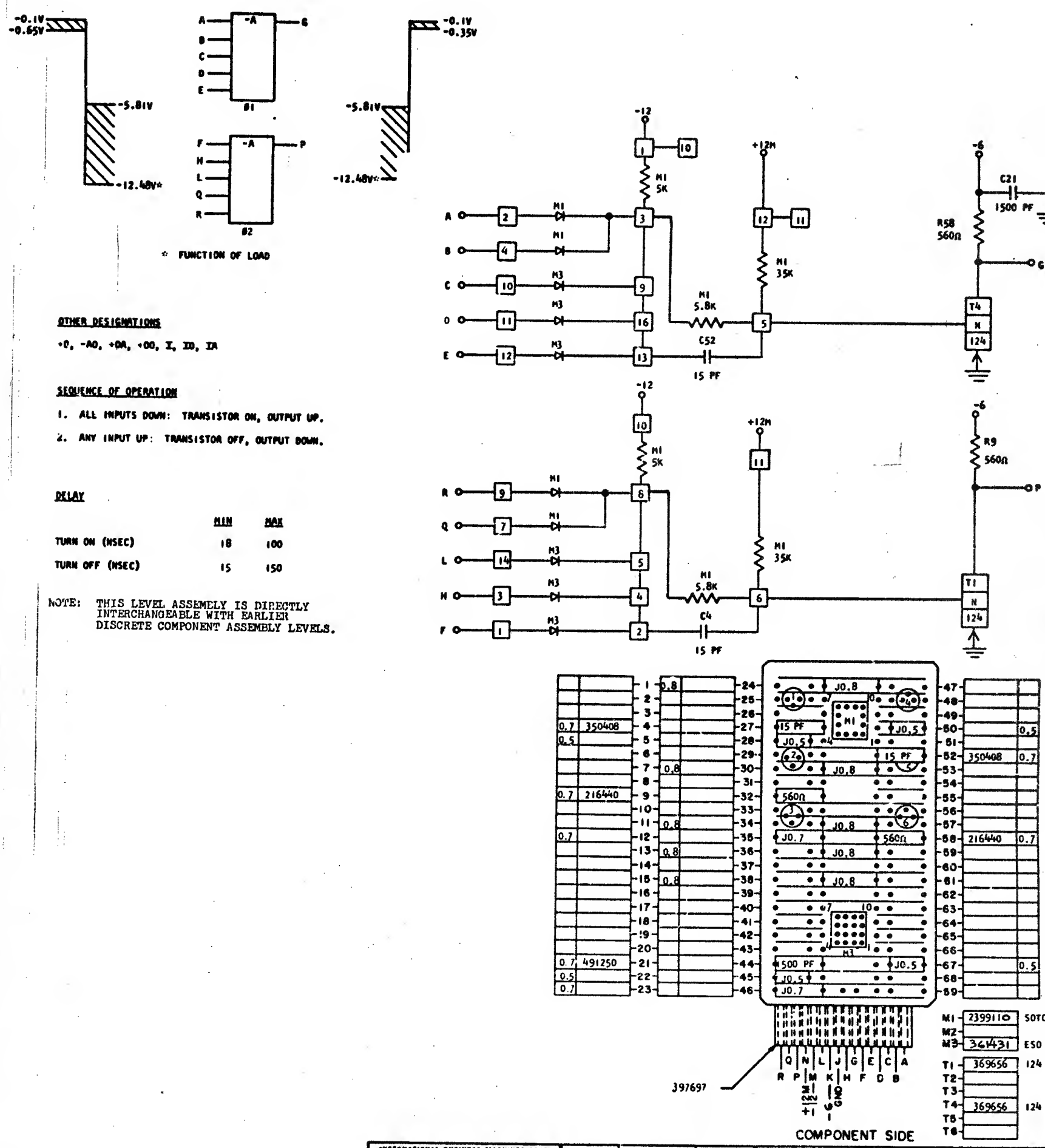
734367

ZGL—

P/N: 372589

REFERENCE DRAWING
PRODUCTION DRAWING 372589

SDTDL HS TWO 5-WAY NEGATIVE AND LOGIC BLOCKS WITH LOADS



☆ FUNCTION OF LOAD

OTHER DESIGNATIONS

+0, -A0, +0A, +00, I, II, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	18	100
TURN OFF (NSEC)	15	150

NOTE: THIS LEVEL ASSEMELY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	SDTDL HS TWO 5-WAY NEGATIVE AND LOGIC BLOCKS WITH LOADS				
DESIGN			MODEL	SMS	
DETAIL			SCALE	NONE	
CHECK			DRAW	MDE	4-16-63
APPRO		4-24-63	CHECK		

DATE	CHANGE NO.	APPROVAL
4-24 63	116800C	
24 JAN 66	126401D	
1 APR 66	126401J	GLK
	132172	

DATE	CHANGE NO	APPROVAL

DEVELOPMENT NO.

734367

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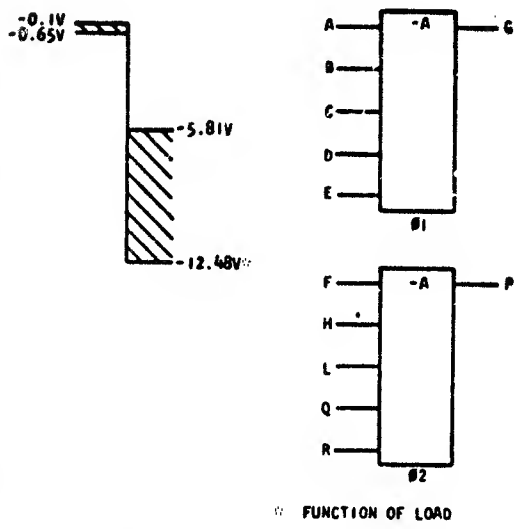
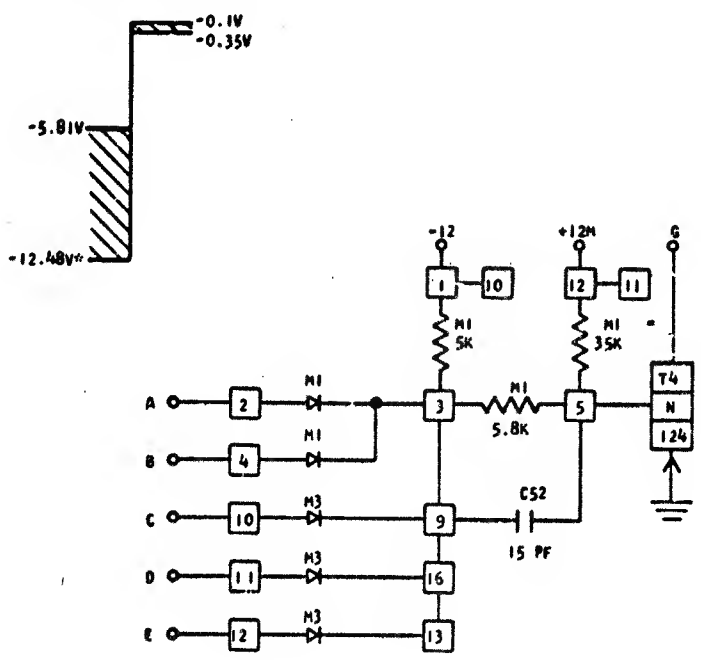
P/N: 372590

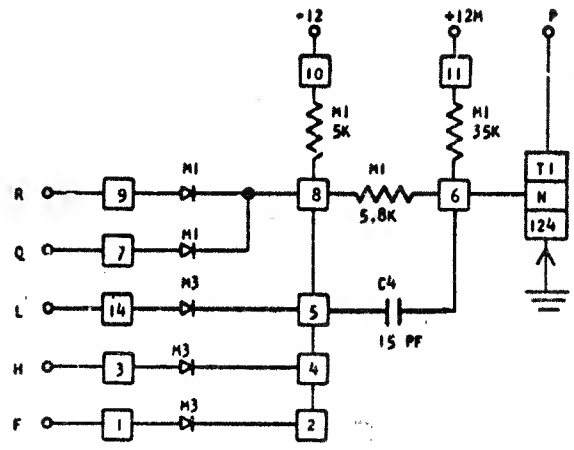
REFERENCE DRAWING
PRODUCTION DRAWING 372590

SDTDL HS TWO 5-WAY NEGATIVE AND LOGIC BLOCKS WITHOUT LOADS



☆ FUNCTION OF LOAD





OTHER DESIGNATIONS

-0, -A0, -0A, -00, I, I0, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

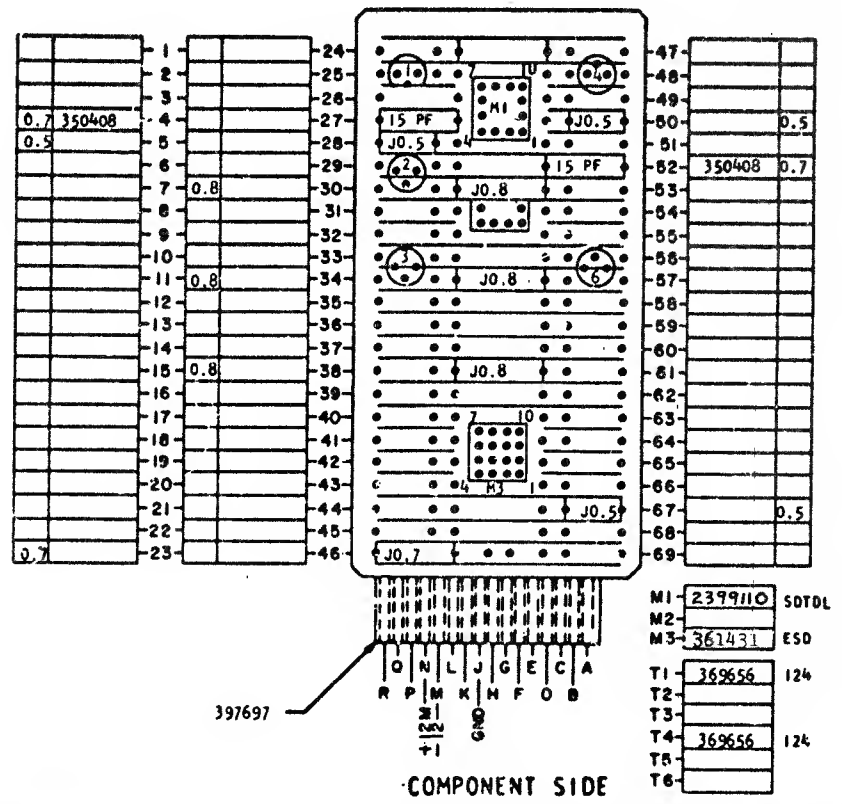
DELAY

WITH 560Ω OR 1.6K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	18	100☆
TURN OFF (NSEC)	15	150☆☆

☆ THIS DELAY CAN INCREASE TO 180 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.
☆☆ THIS DELAY CAN INCREASE TO 200 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

NOTE: THIS LEVEL ASSEMBLY IS DIRECTLY INTERCHANGEABLE WITH EARLIER DISCRETE COMPONENT ASSEMBLY LEVELS.



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	SDTDL HS TWO 5-WAY NEGATIVE AND LOGIC BLOCKS WITHOUT LOADS					4 24-63	116800C						734300
DESIGN			MODEL	SMS 1440		24JAN66	126401D	AKK					
DETAIL			SCALE	NONE		1 APR66	126401J	GLK					
CHECK			DRAW	MDE	4-16-63		132173						
APPRO	[illegible]	4-24-63	CHECK										

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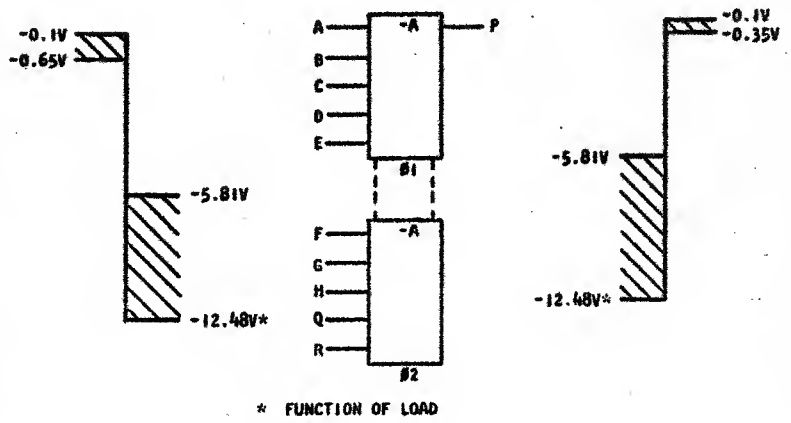
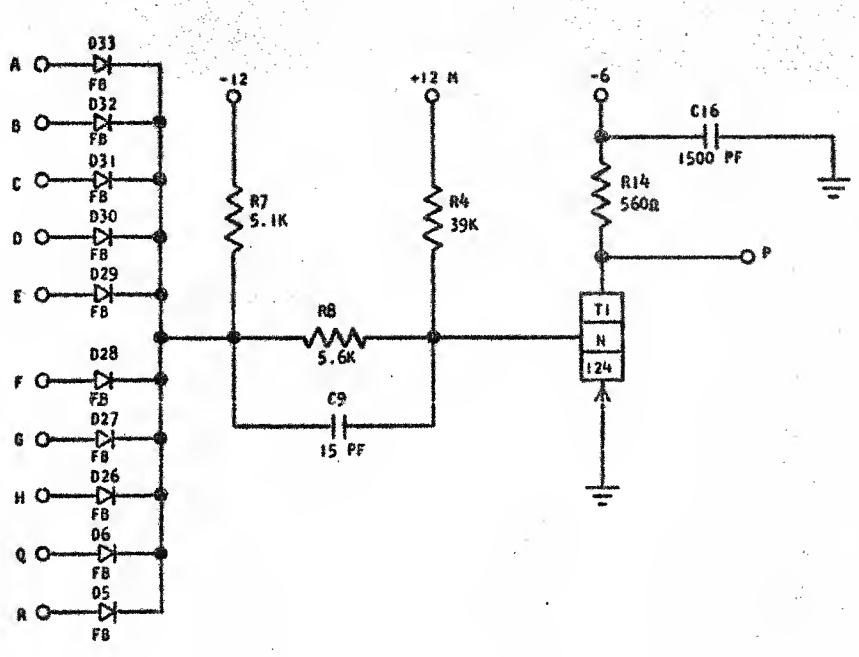
REFERENCE DRAWING
PRODUCTION DRAWING 372591

HS ONE 10-WAY NEGATIVE AND LOGIC BLOCK WITH LOAD



* FUNCTION OF LOAD



OTHER DESIGNATIONS

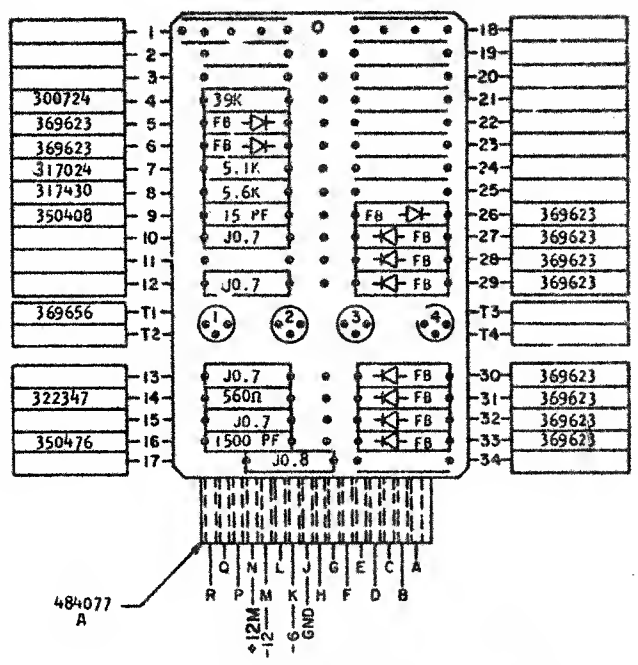
+0, -A0, +0A, +00, I, I0, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	18	100
TURN OFF (NSEC)	15	150



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	HS ONE 10-WAY NEG. AND LOGIC BLOCK WITH LOAD				4-24-63	116800C					
DESIGN			MODEL	SMS 1440	12-30-63	119217					
DETAIL			SCALE	NONE							
CHECK			DRAW	HDE 4-16-63							CIRCUIT FAMILY
APPRO		4-24-63	CHECK								SDTDL

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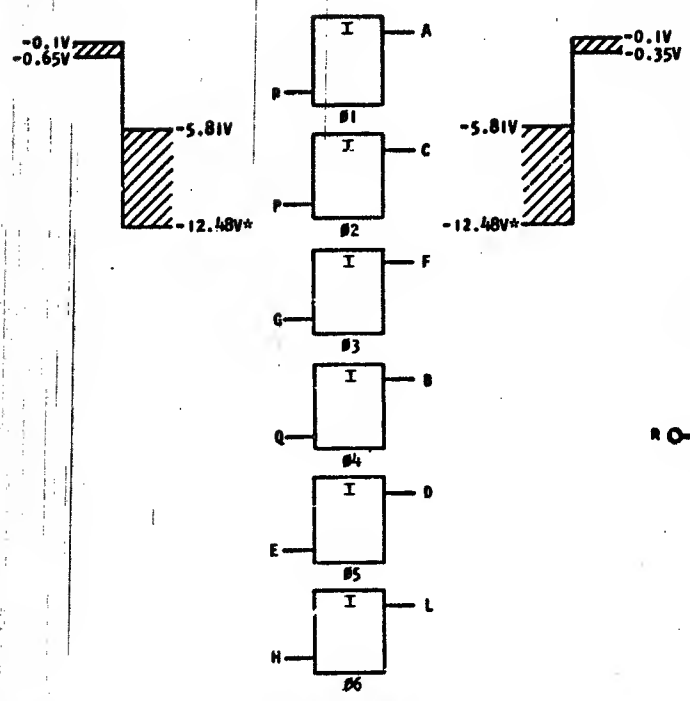
ZGP—

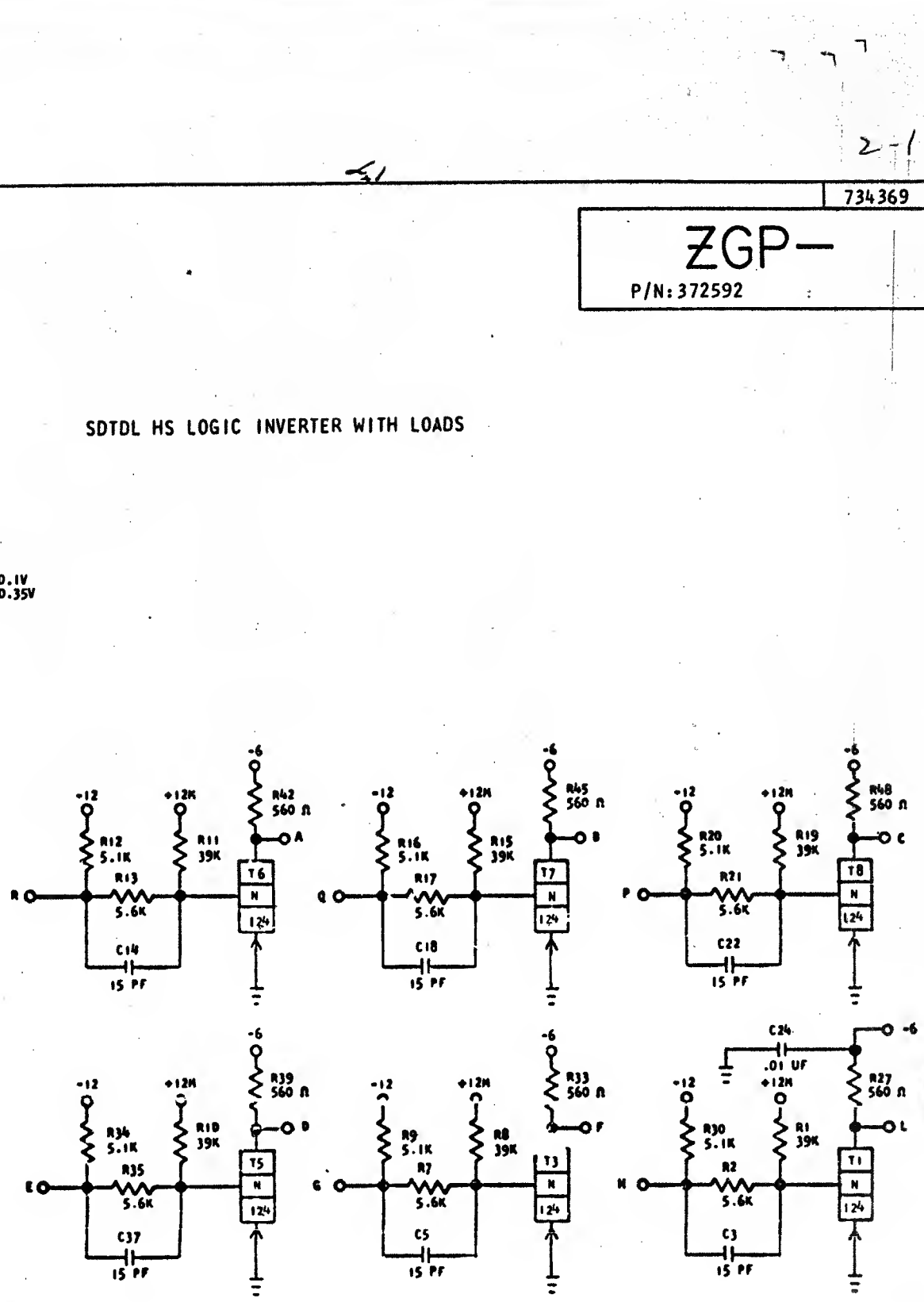
P/N: 372592

REFERENCE DRAWING
PRODUCTION DRAWING 372592

SDTDL HS LOGIC INVERTER WITH LOADS



* FUNCTION OF LOAD



OTHER DESIGNATIONS

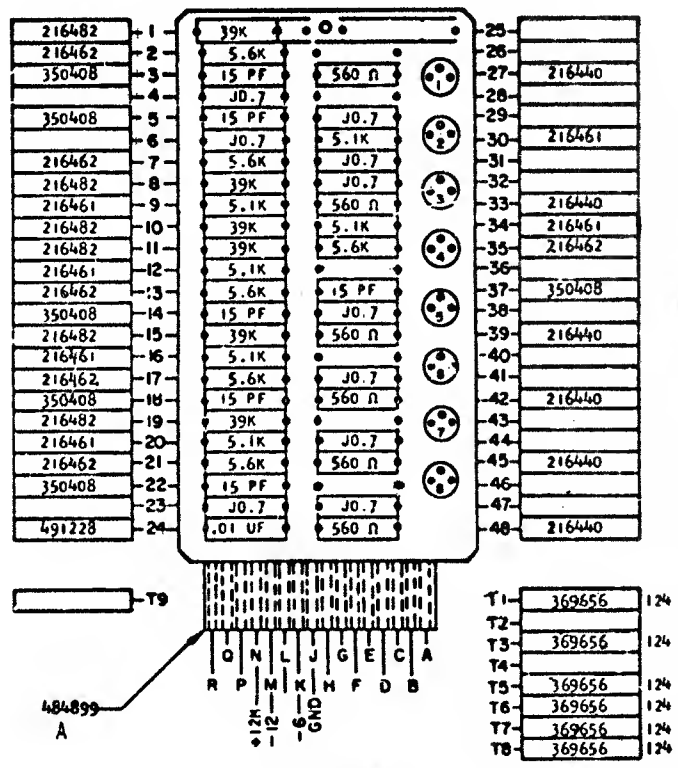
ID, IA

SEQUENCE OF OPERATION

1. INPUT DOWN: TRANSISTOR ON, OUTPUT UP.
2. INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	18	100
TURN OFF (NSEC)	15	150



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL HS LOGIC INVERTER WITH LOADS				4-24-63	116800C					734369
					24JAN66	126401D	JZK				
DESIGN			MODEL	SMS 1440							
DETAIL			SCALE	NONE							
CHECK			DRAW	MDE 4-16-63							
APPRO			CHECK								

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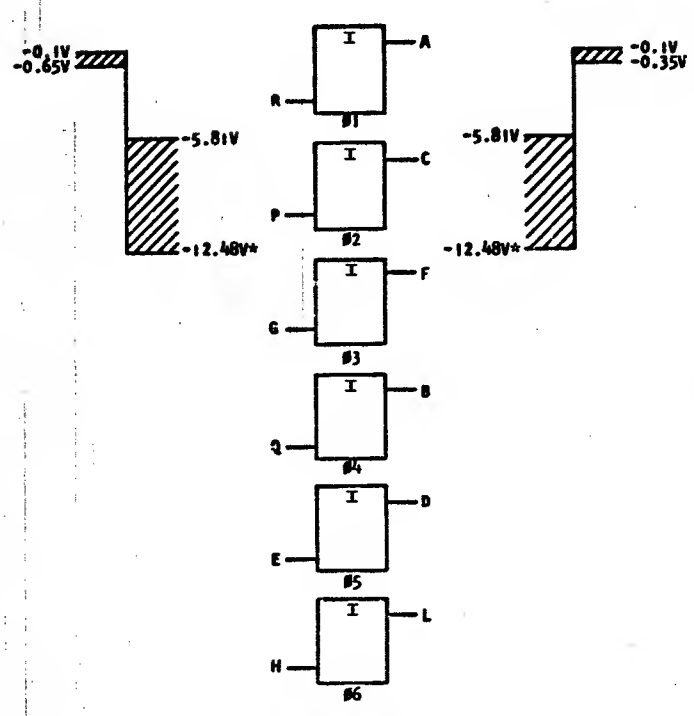
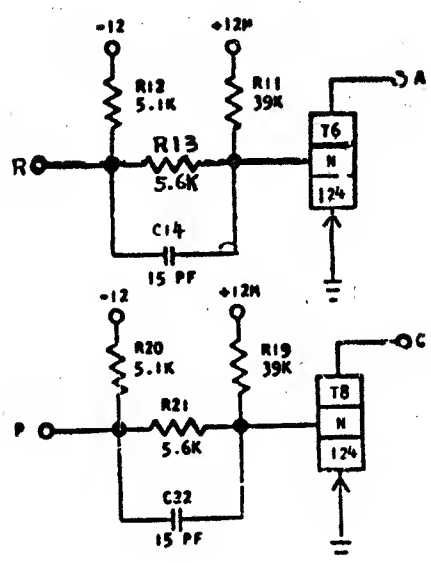
P/N: 372593

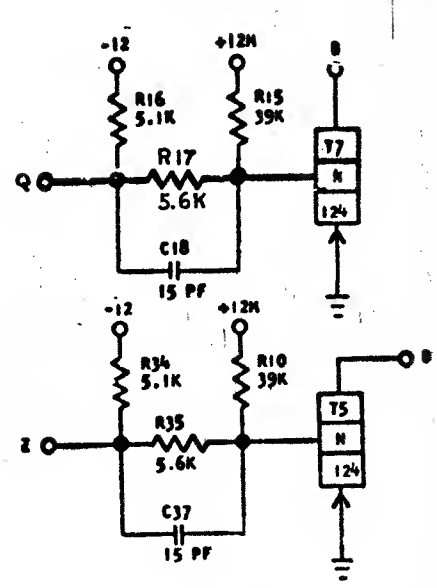
REFERENCE DRAWING
PRODUCTION DRAWING 372593

SDTDL HS LOGIC INVERTER WITHOUT LOADS



* FUNCTION OF LOAD





OTHER DESIGNATIONS

ID, IA

SEQUENCE OF OPERATION

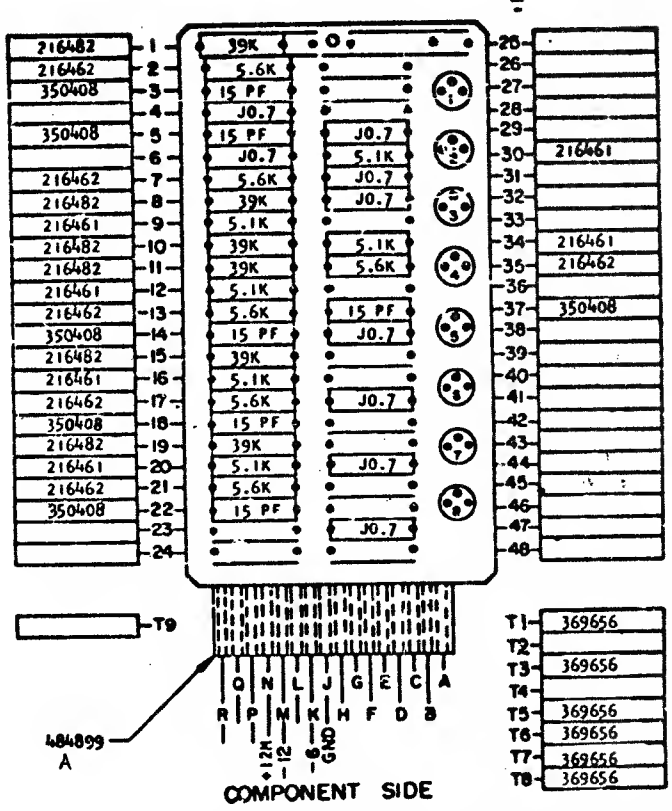
1. INPUT DOWN: TRANSISTOR ON, OUTPUT UP.
2. INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

WITH 560Ω OR 1.6K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	18	100*
TURN OFF (NSEC)	15	150**

* THIS DELAY CAN INCREASE TO 180 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.
** THIS DELAY CAN INCREASE TO 200 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL HS LOGIC INVERTER WITHOUT LOADS				4-24-63	116800C					734370
DESIGN			MODEL	SMS 1440	24JAN66	126401D	AZK				
DETAIL			SCALE	NONE							
CHECK			DRAW	MOE 4-16-63							
APPRO	REF	4-24-63	CHECK								

C

2-1

STANDARDS CODE	2-7045

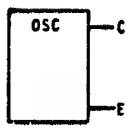
734384

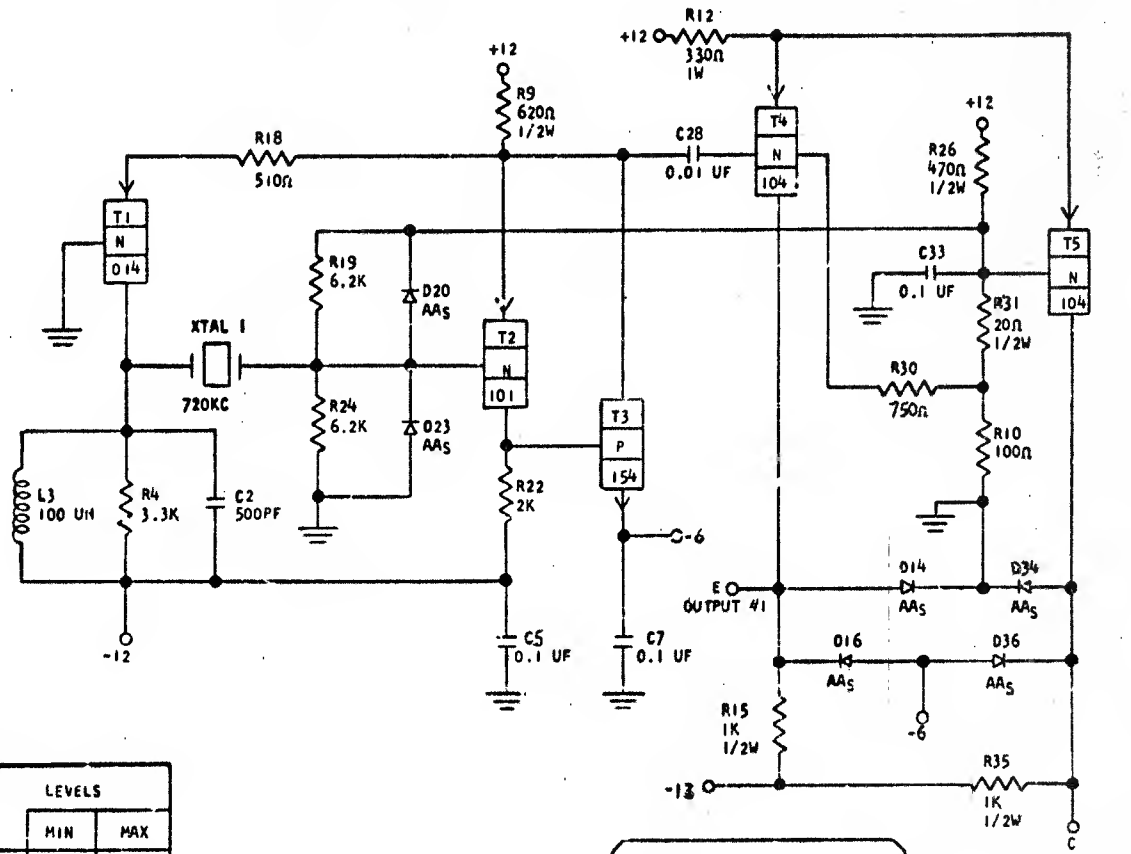
CARD CODE	734384
Z K T -	

REFERENCE DRAWING

PRODUCTION DRAWING 372682

720 KC OSCILLATOR AND SHAPER

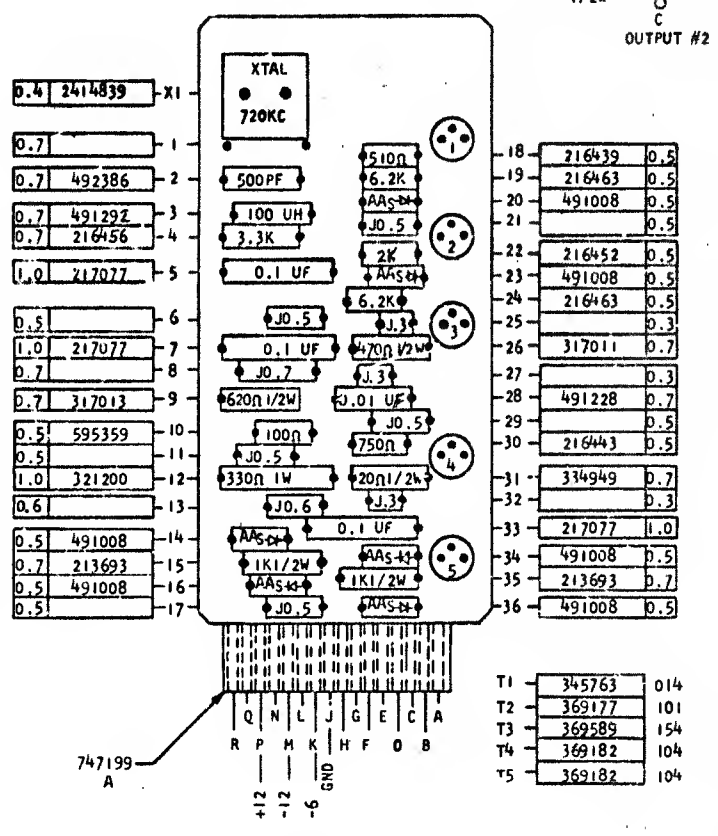




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.

PINS	SIGNAL NAME		WAVESHAPE		LEVELS MIN	LEVELS MAX
C	Y	OUTPUT #2		UP	0.0V	+0.5V
				DOWN	-5.86V	-6.64V
E	Y	OUTPUT #1		UP	0.0V	+0.5V
				DOWN	-5.86V	-6.64V



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
NAF	10-1-62

INTERNATIONAL BUSINESS MACHINES CORP.														
NAME	720 KC OSCILLATOR AND SHAPER													
DESIGN			MODEL	SMS 1441/1461										
DETAIL			SCALE	NONE										
CHECK	JAB 7-22-63		DRAW	JAB	7-22-63									
APPRO	[illegible] 8-1-63		CHECK	[illegible]	7-23-63									

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
8-5-63	117827					
12-29-64	120699	GLK				
14OCT65	125832					

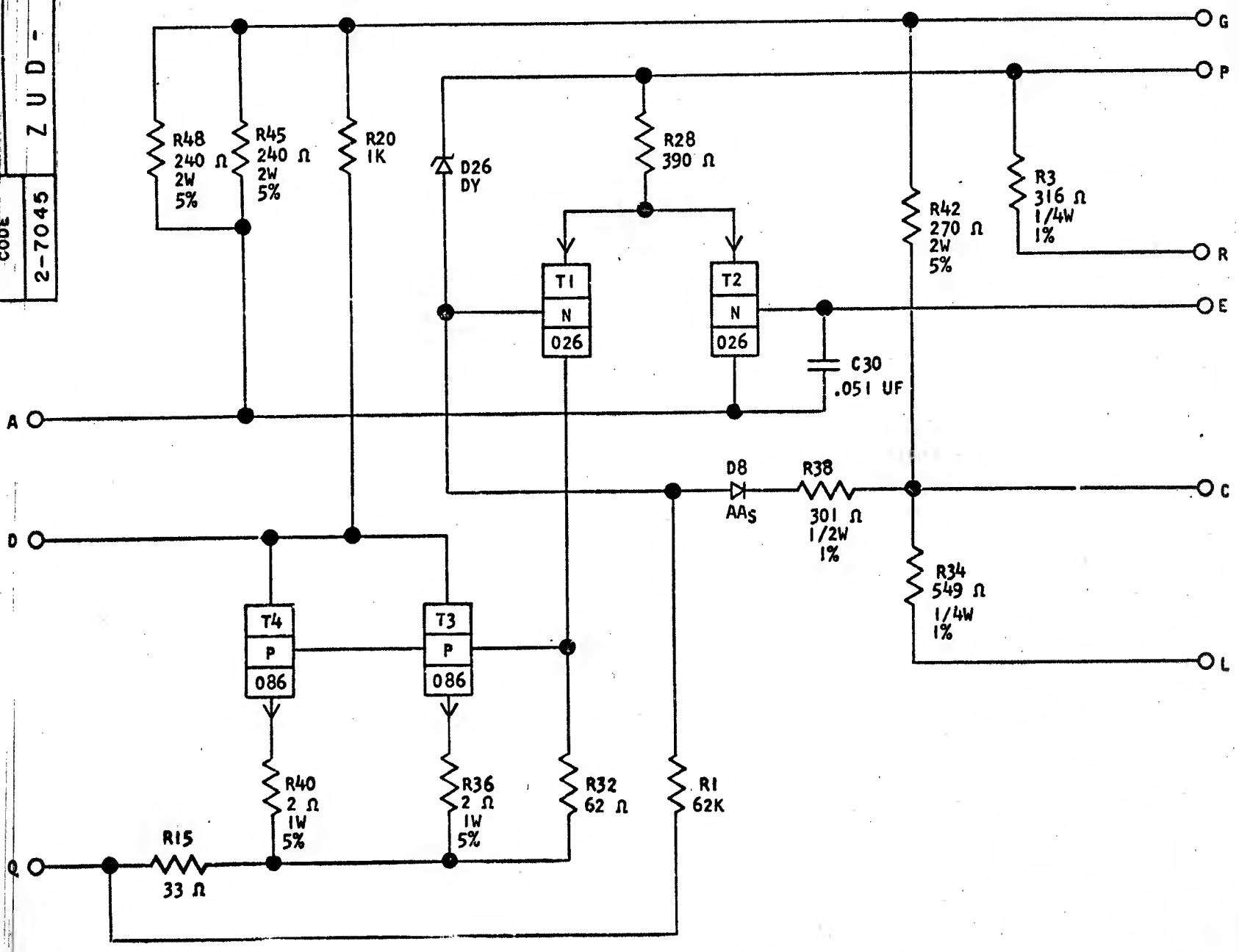
734384

C

12V AMPLIFIER CARD FOR MPS POWER SUPPLY

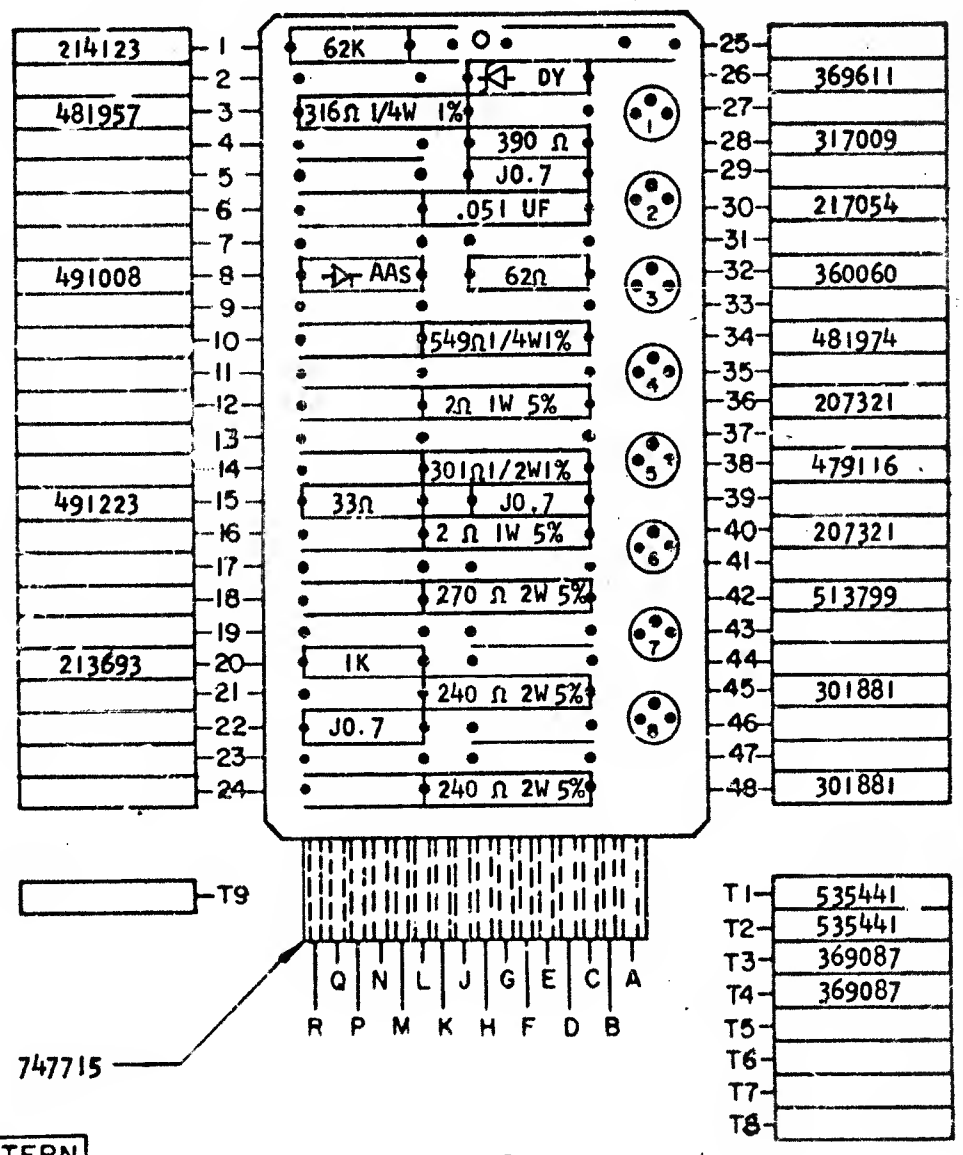
372085

STANDARDS CODE 2-7045 — 372085 — Z U D -



NOTES

- X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 870085
- XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
- XII ALL RESISTORS ARE 1/2 WATT AND ± 5% UNLESS OTHERWISE NOTED
- XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296



COMPONENT SIDE

B

CIRCUIT AND PACKAGING STANDARD											
APPROVAL		DATE		HOLE PATTERN							
GDS		12-11-63		493457							
INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	372085
NAME	CARD ASM TSTR-12V AMPLIFIER CARD FOR MPS POWER SUPPLY			1-24-64	119699					K110043	
DESIGN	RCB	12-63	MODEL	SMS 1051							
DETAIL	RAT	12-63	SCALE	NONE							
CHECK	JJ	12-63	DRAW	HTD 11-5-63						CIRCUIT FAMILY	
APPRO	REB	12-63	CHECK							SPECIAL	